MB86S72 Data sheet

Version 1.40
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Revision History

Date	Version	Description of revision	Approved by	Inspected by	Prepared by
2015/5/20	1.00	First Revision	Nakahara	Endo	Nakanishi
2015/5/29	1.10	Corrected typos, omissions, and incorrect descriptions In 2.6.2.2. PRMUX register 3'h1 of 2. 6. Pin Sharing UART#0: Some reserved dedicated pins were clearly specified as "Not used."	Nakahara	Endo	Nakanishi
2015/6/3	1.20	Corrected incorrect descriptions in 3.5.4 eMMC and 3.5.9 SDIO	Nakahara	Endo	Nakanishi
2015/11/12	1.30	Added a condition in 3.5.9. SDIO Signal Timing (3.5.9.3. Output Signal)	Nakahara	Endo	Nakanishi
2017/4/25	1.40	Renewd Figure 2-1 to make it easy to see.	Nakahara	Endo	Yoshikawa

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CONTENTS

1. Overview

This chapter describes an overview of MB86S72.

1.1. Features

- MB86S72
  - The Cortex®-A15 processor operating at 1600MHz (max) and the Cortex®-A7 processor operating at 1200MHz (max) are installed, which allows the big.LITTLE™ processing to provide high performance and high power-efficiency.
  - Hardware coherent organization based on a cache coherent bus is installed. Consistency of shared data is ensured by hardware. Realized software load and power saving.
  - Various high-speed interfaces and memory interfaces are installed, which makes it possible to handle various applications such as all-in-one devices, industrial equipment, and multimedia devices.
- Advanced Power Management
  - Power Down, Clock Gating, and Clock Gear Down for each block
  - DVFS allows a processor to control the power carefully
  - Fine power supply control by PMU (Power Management Unit)
  - A temperature sensor is installed, which allows the temperature of each processor and DDR controller unit to be monitored
  - Network standby answer mode
    - Major sections can be powered down while maintaining the network connection by the proxy answering macro
    - Fine controls of proxy answer and recovery are possible due to the original filter processing.
- 2D/3D Graphics Controller
  - High performance graphic accelerator ARM® Mali™-T624
    - Compatible with Visual Computing in a wide range of fields
    - Processor ideally suitable for GPGPU (General Purpose computing on GPU)
    - Industry standard APIs of OpenGL ES1.1/2.0/3.0 and OpenCL1.1 are supported.
    - Single core, L2 Cache=32KB
  - 2D dedicated engine installed
- Cortex®-A15 Processor Core
  - Maximum operation frequency: 1600MHz
  - Dual-core
  - NEON™ SIMD high performance media engine
  - L1Cache I/D = 32KB/32KB, L2 Cache = 1 MB
- Cortex®-A7 Processor Core
  - Maximum operation frequency: 1200MHz
  - Dual-core
  - NEON™ SIMD high performance media engine
  - L1Cache I/D = 32KB/32KB, L2 Cache = 512KB
- System Controller
  - Cortex®-M3 is installed, realizing flexible boot control, clock control, and power supply control

- Memory Controllers
  - DDR3/DDR3L SDRAM
    - Maximum frequency 1600MHz (DDR3) / 1333MHz (DDR3L)
      * The maximum transfer rate that can be realized varies depending on the DRAM configuration and the board characteristics.
    - Connection topology: DIMMx1, DIMMx2, DIMM+OnBoard, OnBoard
    - Data width 64-bit/32-bit
    - Maximum memory capacity 8GB (for 64-bit data width)/4GB (32-bit)
    - Complies with maximum 4 Ranks
    - DIMM supported
  - NOR FLASH
    - 2 chip selects
    - 16-bit/8-bit data bus width
    - Timing setting and data bus width that can be programmed for each chip select.
  - NAND FLASH
    - 2 chip selects
    - 16-bit/8-bit data bus width
    - Timing setting and data bus width that can be programmed for each chip select.
  - Serial Flash
    - 2 chip selects
    - 1-bit (single), 2-bit (dual), and 4-bit (quad) data widths supported
- JPEG codec
  - JPEG baseline and M-JPEG decoding and encoding
  - JPEG Baseline ISO/IEC 10918-1 compliant
  - Supported formats: 4:2:0, 4:2:2, 4:4:0, 4:4:4, 4:0:0
  - Maximum resolution 32768x32768
  - Maximum 1270Mbit/s (encode), 1184Mbit/s (decode) (during 4:2:2)
- Audio Interfaces
  - I2S interface (2 Ch: I/O independent)
- Display Interfaces
  - LCD interface
    - 1 FPDlink (LVDS)
    - VESA/JEIDA formats supported
    - 4 pairs
    - Maximum 81MHz
- Ethernet Media Access Controller
  - IEEE802.3-2005 compliant
  - 10/100/1000Mbps
  - RGMII interface
  - IEEE802.3az-2010 (Energy Efficiency Ethernet) compliant
- SDIO
  - Supports SD cards conforming to the following standards
    - Part 1 Physical Layer Specification version 3.01
    - Part E1 SDIO Specification version 3.00
    - Part A2 SD Host Controller Standard Specification 3.00
  - SDR50, SDR104, DDR50 modes supported
- eMMC Controller
  - eMMC4.51 compliant
  - High Speed SDR, High Speed DDR, HS200 modes supported

- High Speed Interface
  - PCI-express
    - 3 controllers + 8 SerDes
      Available Lane combinations
      x4+x2+x2, x4+x2+x1, x4+x1+x1, x2+x2+x2, x2+x2+x1, x2+x1+x1, x1+x1+x1,
      x4+x4, x4+x2, x4+x1, x2+x2, x2+x1, x1+x1, x4, x2, x1
    - Link width can be set in the Link Capabilities Register
    - Each port supports Gen1 (2.5GT/s) and Gen2 (5.0GT/s)
    - Root or Endpoint selection is possible in each port
  - USB3.0 Host Controller
    - xHCI compliant USB3.0 host controller
    - 2 Channels installed
    - Super Speed (5Gbps), High Speed (480Mbps), Full Speed (12Mbps), and Low Speed (1.5Mbps) are supported
    - xHCI PC authentication supported (USB3.0 #0 port <-> PCI-express #0 port)
  - USB2.0 Host Controller
    - EHCI1.0 and OHCI1.0a are supported
    - 1 Channel installed
    - High Speed (480Mbps), Full Speed (12Mbps), and Low Speed (1.5Mbps) are supported
  - USB2.0 Host/Device Controller
    - Host/Device selectable USB controller
    - 1 Channel installed
    - High Speed (480Mbps), Full Speed (12Mbps), and Low Speed (1.5Mbps) are supported
- Peripherals
  - UART
    - 16C650 equivalent serial interface
    - 8-wire, 4-wire, and 2-wire formats supported.
    - Hardware flow control supported
  - I2C
    - Standard Mode (maximum 100Kbps), Fast mode (maximum 400Kbps): 3 channels
      - Master transmit/receive function
      - Slave transmit/receive function
      - Arbitration function
      - Clock synchronization function
      - Slave address detection function (only 7-bit is supported, 10-bit is not supported)
      - General call address detection function (the detection function is restricted in the master mode)
      - Transfer direction detection function
      - Repeated start condition generation and detection function
      - Bus error detection function
      - CBUS standard not supported
    - Standard Mode (max 100Kbps), Fast mode (max 400Kbps), Hs mode (max 2Mbps): 2 channels
      - Master transmit/receive function
      - Iterative start condition generation function
      - Bus error detection function
      - CBUS standard not supported
      - Only the single master function is supported. Slave function and multi-master function are not supported
  - GPIO
    - 66-bit general purpose input/output port (shared with other signals)

- IO drive power selection function
- External interrupts
  - Max. 32 interrupts (shared with GPIO)

- Security
  - Secure boot (NOR FLASH, Serial FLASH)
  - ARM® TrustZone® Technology compliant
- Advanced Multi Core Debug
  - Multi-core debug system compatible with the CoreSight™ architecture
  - Real time trace by ETM
  - 64KB trace buffer and max 16-bit trace port
  - Embedded Cross Triggering
  - JTAG and SWD (Serial Wire Debug) are supported

1.2. Block Diagram

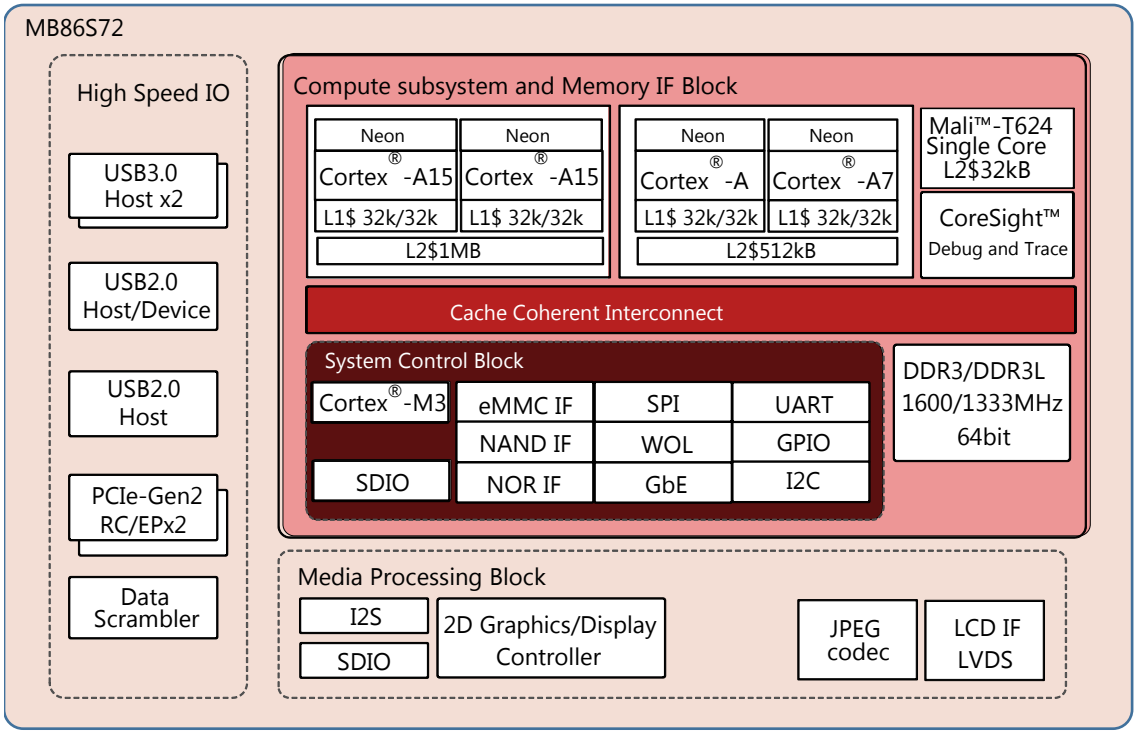

Figure 1-1: Block Diagram

2. Package and Pin Information

2.1. Package Outline Drawing

The package information is shown below.

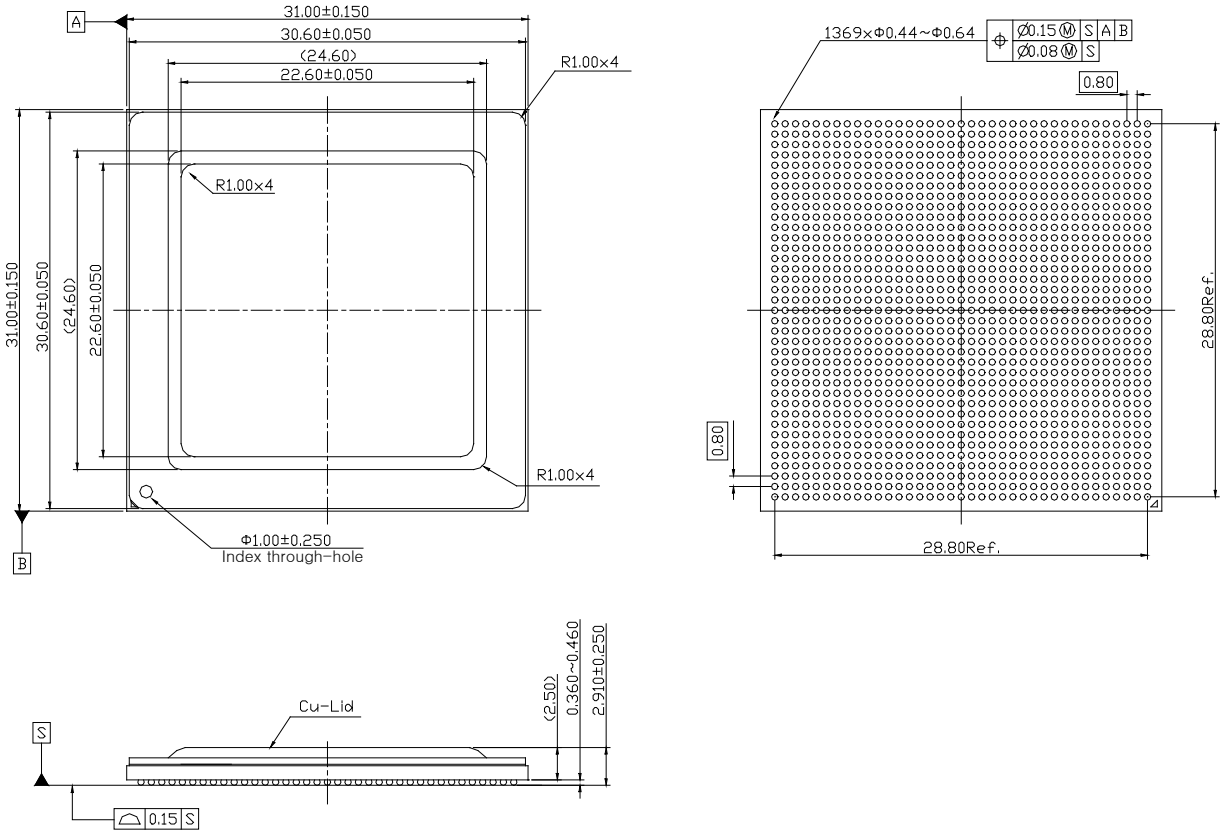

Figure 2-1: Package Outline Drawing

2.2. Ball Assignment

The ball assignment is shown below.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	
37	AVS_USB2H	USB2H_DP	AVS_USB2H	AVS_USB2HDC	USB2D_DP	AVS_USB2HDC	VSU_USB30	USB30_SSEARXP	VSN_USB30	USB30_SSEXTXOP	AVS_USB30	USB30_HSDP	AVS_USB30	VSU_USB31	USB31_SSEARXP	VSN_USB31	USB31_SSEXTXOP	AVS_USB31	USB31_HSDP	USB3_REFCLK	GD_PCIE	PCIE0_RXP0	GD_PCIE	PCIE0_RXP1	GD_PCIE	PCIE0_RXP2	GD_PCIE	PCIE0_RXP3	GD_PCIE	PCIE1_RXP0	GD_PCIE	PCIE1_RXP1	GD_PCIE	PCIE1_RXP2	GD_PCIE	PCIE1_RXP3	GD_PCIE	37
36	AVS_USB2H	USB2H_DM	AVS_USB2H	AVS_USB2HDC	USB2D_DM	AVS_USB2HDC	VSU_USB30	USB30_SSEARXN	VSN_USB30	USB30_SSEXTXON	AVS_USB30	USB30_HSDM	AVS_USB30	VSU_USB31	USB31_SSEARXN	VSN_USB31	USB31_SSEXTXON	AVS_USB31	USB31_HSDM	AVS_USB31	GD_PCIE	PCIE0_RXN0	GD_PCIE	PCIE0_RXN1	GD_PCIE	PCIE0_RXN2	GD_PCIE	PCIE0_RXN3	GD_PCIE	PCIE1_RXN0	GD_PCIE	PCIE1_RXN1	GD_PCIE	PCIE1_RXN2	GD_PCIE	PCIE1_RXN3	GD_PCIE	36
35	AVS_USB2H	AVS_USB2H	AVS_USB2H	AVS_USB2HDC	AVS_USB2HDC	AVS_USB2HDC	VSU_USB30	VSU_USB30	VSN_USB30	VSN_USB30	AVS_USB30	AVS_USB30	AVS_USB30	VSU_USB31	VSU_USB31	VSN_USB31	VSN_USB31	AVS_USB31	AVS_USB31	AVS_USB31	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	35
34	AVDF1_USB2H	AVDF1_USB2H	AVDF2_USB2H	AVDF1_USB2HDC	AVDF1_USB2HDC	AVDF2_USB2HDC	VDU_USB30	VDU_USB30	VDN_USB30	VDN_USB30	AVDF1_USB30	AVDF1_USB30	AVDF2_USB30	VDU_USB31	VDU_USB31	VDN_USB31	VDN_USB31	AVDF1_USB31	AVDF1_USB31	AVDF2_USB31	GD_PCIE	PCIE0_REFCLKP1	GD_PCIE	PCIE0_TXPO0	PCIE0_TXPO1	GD_PCIE	PCIE0_TXPO2	PCIE0_TXPO3	GD_PCIE	PCIE1_TXPO0	PCIE1_TXPO1	GD_PCIE	PCIE1_TXPO2	PCIE1_TXPO3	GD_PCIE	PCIE1_REFCLKP1	GD_PCIE	34
33	AVS_USB2H	AVS_USB2H	AVS_USB2H	AVS_USB2HDC	AVS_USB2HDC	AVS_USB2HDC	VSU_USB30	VSU_USB30	VSN_USB30	VSN_USB30	AVS_USB30	AVS_USB30	AVS_USB30	VSU_USB31	VSU_USB31	VSN_USB31	VSN_USB31	AVS_USB31	AVS_USB31	AVS_USB31	GD_PCIE	PCIE0_REFCLKM1	GD_PCIE	PCIE0_TXNO0	PCIE0_TXNO1	GD_PCIE	PCIE0_TXNO2	PCIE0_TXNO3	GD_PCIE	PCIE1_TXNO0	PCIE1_TXNO1	GD_PCIE	PCIE1_TXNO2	PCIE1_TXNO3	GD_PCIE	PCIE1_REFCLKM1	GD_PCIE	33
32	AVD18_USB2H	AVD18_USB2H	AVDF2_USB2H	AVD18_USB2HDC	AVD18_USB2HDC	AVDF2_USB2HDC	VDU_USB30	VDU_USB30	VDN_USB30	VDN_USB30	AVD18_USB30	AVD18_USB30	AVDF2_USB30	VDU_USB31	VDU_USB31	VDN_USB31	VDN_USB31	AVD18_USB31	AVD18_USB31	AVDF2_USB31	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	32
31	AVSP_USB2H	AVSP_USB2H	AVS_USB2H	AVSP_USB2HDC	AVSP_USB2HDC	AVS_USB2HDC	VSU_USB30	VSU_USB30	VSN_USB30	VSN_USB30	AVSP_USB30	AVSP_USB30	AVS_USB30	VSU_USB31	VSU_USB31	VSN_USB31	VSN_USB31	AVSP_USB31	AVSP_USB31	AVS_USB31	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	VPTX_PCIE0	VPTX_PCIE0	VPTX_PCIE0	VPTX_PCIE0	GD_PCIE	VPTX_PCIE1	VPTX_PCIE1	VPTX_PCIE1	VPTX_PCIE1	VPTX_PCIE1	GD_PCIE	GD_PCIE	GD_PCIE	31
30	AVDP_USB2H	AVDP_USB2H	USB2H_EXT12K	AVDP_USB2HDC	AVDP_USB2HDC	USB2D_EXT12K	VDU_USB30	VDU_USB30	VDN_USB30	VDN_USB30	AVDP_USB30	AVDP_USB30	USB30_HSEXT12K	VDU_USB31	VDU_USB31	VDN_USB31	VDN_USB31	AVDP_USB31	AVDP_USB31	USB31_HSEXT12K	GD_PCIE	GD_PCIE	GD_PCIE	GD_PCIE	VPH_PCIE0	VPH_PCIE0	PCIE0_REFRES_I	VP_PCIE0	VP_PCIE0	GD_PCIE	VPH_PCIE1	VPH_PCIE1	PCIE1_REFRES_I	VP_PCIE1	VP_PCIE1	GD_PCIE	GD_PCIE	GD_PCIE	30
29	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	29
28	XUSB2D_OVCRNTI			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVS_PLL7	AVS_PLL8	AVSH_CA7_0	AVSH_CA7_1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DDR_DTO1	DDR_ATO	VSS	DDR_DQ0	DDR_DQ2	DDR_DQ1	DDR_DQM0	28
27	USB30_VBUSCTRL	USB2D_VBUSVALI	USB2D_DPUO	VSS	USB2D_IDDIGI	VSS	VSS	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	AVD_PLL7	AVD_PLL8	AVDH_CA7_0	AVDH_CA7_1	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	DDR_DTO0	VSS	DDR_DQ3	VSS	DDR_DQ5	XDDR_DQS0	DDR_DQS0	27
26	USB2H_PRTPWRO	USB30_OVERCRNT	USB31_OVERCRNT	XUSB2H_OVCRNTI	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDE15	VSS	VDE15	VSS	VSS	DDR_DQ7	VSS	DDR_DQ4	DDR_DQ6	VSS	DDR_DQ13	26
25	USB31_VBUSCTRL	USB2D_PRTPWRO	XPCIE1_X4_PERST	VSS	X4_PRVRETYPE	AVS_PLL2	AVD_PLL2	VDE	VDE	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_CA7	VDD_CA7	VDD_CA7	VDD_CA7	VDD	VDD	VDD	VDD	VDE15	VSS	VDE15	VSS	VDE15	DDR_DQ8	VSS	DDR_DQ10	VSS	DDR_DQ11	XDDR_DQS1	DDR_DQS1	25
24	XPCIE1_X2_PERST	XPCIE0_PERST	PCIE1_X2_PRVRETYP	PCIE0_PRVRETYPE	VSS	AVSH_CA15_1	AVDH_CA15_1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VAA_PLL1	VSS	VDE15	VSS	VDE15	VSS	DDR_DQ9	VSS	DDR_DQM1	DDR_DQ12	DDR_DQ14	DDR_DQ15	24
23	XTRST	TDO	TDI	VSS	XSRST	AVSH_CA15_0	AVDH_CA15_0	VDE	VDE	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_CA7	VDD_CA7	VDD_CA7	VDD_CA7	VDD	VDD	VDD	VSS	VDE15	VSS	VDE15	VSS	VDE15	DDR_DQ17	VSS	DDR_DQ18	VSS	DDR_DQ19	DDR_DQ16	DDR_DQM2	23
22	SCLKCA7	VSS	TMS	TCK	VSS	AVS_PLL1	AVD_PLL1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	DDR_DQ21	VSS	DDR_DQ20	DDR_DQ22	XDDR_DQS2	DDR_DQS2	22
21	I2C4_SDA	I2C3_SDA	I2C4_SCL	VSS	VSS	VSS	VSS	VDE	VDE	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA7	VDD_CA7	VDD_CA7	VDD_CA7	VDE15	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	VDE15	DDR_DQ23	VSS	DDR_DQM3	VSS	DDR_DQ26	VSS	DDR_DQ27	21
20	I2C3_SCL	I2C2_SCL	I2C1_SDA	I2C0_SCL	VSS	PD56	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	DDR_MZQRES	VSS	DDR_DQ25	VSS	DDR_DQ24	DDR_DQ30	XDDR_DQS3	DDR_DQS3	20
19	I2C1_SCL	I2C0_SDA	I2C2_SDA	VSS	PD57	VSS	PD47	VDE	VDE	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA7	VDD_CA7	VDD_CA7	VDD_CA7	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	DDR_MVREF	XDDR_RESET	VSS	DDR_DQ31	VSS	DDR_DQ28	DDR_DQ29	DDR_DQ_KE0	19
18	SCLKCA15	VSS	PD63	PD58	VSS	PD48	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	VDE15A	VSS	DDR_CKE2	VSS	DDR_CKE3	DDR_ADD15	DDR_ADD14	DDR_CKE1	18
17	PD65	PD62	PD59	VSS	PD49	VSS	PD37	VDE	VDE	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD_CA15	VDD	VDD	VDD	VDD	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	DDR_BA2	VSS	DDR_ADD12	VSS	DDR_ADD9	DDR_ADD11	DDR_ADD7	17
16	PD64	PD60	PD52	PD50	VSS	PD38	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	VDE15A	VSS	DDR_ADD8	VSS	DDR_ADD6	VSS	XDDR_CLKO0	DDR_CLKO0	16
15	PD61	PD54	PD51	VSS	PD39	VSS	PD28	VDE	VDE	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDE15	VSS	VDE15	VSS	VDE15	VSS	DDR_ADD5	VSS	DDR_ADD4	VSS	DDR_ADD0	XDDR_CLKO1	DDR_CLKO1	15
14	PD55	VSS	PD44	PD40	VSS	PD29	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VAA_PLL2	VDE15	VSS	VDE15	VSS	VDE15	VSS	DDR_ADD3	VSS	DDR_ADD2	VSS	XDDR_CLKO2	DDR_CLKO2	14
13	PD53	PD45	PD41	VSS	PD30	VSS	PD18	VDE	VDE	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD_SCB	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDE15	VSS	VDE15	VSS	VDE15	VSS	DDR_ADD1	VSS	DDR_BA0	VSS	DDR_BA1	XDDR_CLKO3	DDR_CLKO3	13
12	PD46	PD42	PD34	PD31	VSS	PD19	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDE15	VSS	VDE15	VSS	VDE15	VSS	XDDR_CAS	VSS	DDR_ADD10	DDR_ODT0	DDR_ODT3	DDR_ODT2	12
11	PD43	PD35	PD32	VSS	PD20	VSS	PD9	VDE	VDE	VDE	VDE	VDE	VDE	VDE	VDE	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VDE15	VSS	VDE15	VSS	XDDR_RAS	VSS	DDR_ADD13	VSS	XDDR_CS1	XDDR_CS3	XDDR_CS2	11
10	PD36	VSS	PD25	PD21	VSS	PD10	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVS_PLL3	AVSH_DDR	AVSH_MALI	AVS_PLL4	VSS	VSS	VSS	VSS	VSS	VSS	DDR_DQ35	VSS	DDR_DQ33	DDR_DQ32	XDDR_WE	DDR_ODT1	XDDR_CS0	10
9	PD33	PD26	PD22	VSS	PD11	VSS	PD0	VDDA	VDDA	VDDA	VDE	VDE	VDEA	VDEA	VDEA	AVD_PLL5	VDE_SDIO1	VDE_SDIO1	VDE_SDIO0	VDE_SDIO0	AVD_PLL3	AVDH_DDR	AVDH_MALI	AVD_PLL4	VDE2	VDE2	VDE2	VSS	VSS	VSS	DDR_DQ39	VSS	DDR_DQ36	VSS	DDR_DQ34	DDR_DQS4	XDDR_DQS4	9
8	PD27	PD23	PD16	PD12	VSS	PD1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVS_FLL5	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DDR_DQ37	VSS	DDR_DQ38	DDR_DQM4	VSS	DDR_DQ32	8
7	PD24	PD15	PD13	VSS	PD2	VSS	ET_INT	VSS	ET_RXD0	VSS	EMMC_DAT0	VSS	DMS0	VSS	TMSEL5	VSS	VBIASP1	VSS	VBIASP_EXT1	VSS	VBIASP_EXT0	VSS	VBIASP0	VSS	VDE_FPD	VDE_FPD	VDE_FPD	VSS	VSS	VSS	DDR_DQ42	VSS	DDR_DQ43	VSS	DDR_DQ41	DDR_DQS5	XDDR_DQS5	7
6	PD17	VSS	PD6	PD3	VSS	ET_PME	VSS	ET_RXDV	VSS	EMMC_DAT2	VSS	POFFCTL3	VSS	TMSEL6	VSS	PCMODE0	VSS	VNODE_N1	VSS	VSS	VSS	VNODE_N0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DDR_DQ45	VSS	DDR_DQ47	DDR_DQ44	DDR_DQM5	DDR_DQ40	6
5	PD14	PD7	PD4	VSS	ET_MDIO	VSS	ET_RXD3	VSS	EMMC_DAT5	VSS	EMMC_SDRSTN	VSS	DMS1	VSS	TMSEL1	VSS	VBIASN1	VSS	VBIASN_EXT1	VSS	VBIASN_EXT0	VSS	VBIASN0	VSS	VDD_FPD	VDD_FPD	VDD_FPD	VSS	VSS	VSS	DDR_DQ46	VSS	DDR_DQ55	VSS	DDR_DQ51	DDR_DQ48	5
4	PD8	PD5	SIN0	SOUT0	VSS	ET_RXD2	VSS	ET_TXD2	VSS	EMMC_DAT4	VSS	POFFCTL0	VSS	TMSEL2	VSS	PCMODE1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	FPD_DATN3	VSS	FPD_DATN0	VSS	I2S0_SDO	VSS	VSS	DDR_DQ54	VSS	DDR_DQ52	DDR_DQ53	DDR_DQS6	XDDR_DQS6	4
3	XRTS0	HSSPI_DAT1	VSS	XCTS0	ET_TXD1	ET_TXEN	ET_TXD3	ET_RXD1	EMMC_DAT1	EMMC_DAT3	EMMC_SDVCC	POFFCTL1	WAKEUP	TMSEL3	VPD1	VPD0	SDIO1_VSEL	SDIO1_PWRERR	SDIO1_DAT2	SDIO1_DAT3	SDIO0_DAT3	SDIO0_DAT2	SDIO0_PWRERR	SDIO0_VSEL	FPD_DATP3	FPD_DATN2	FPD_DATP0	FPD_CLKN	I2S1_FSYN	I2S0_FSYN	VSS	DDR_DQ61	DDR_DQM7	DDR_DQ57	VSS	DDR_DQM6	DDR_DQ49	3
2	HSSPI_DAT2	VSS	HSSPI_DAT0	HSSPI_CSO1	ET_TXD0	VSS	TESTSEL	EMMC_CMD	EMMC_DAT7	VSS	EMMC_DAT6	POFFCTL4	VSS	TMSEL4	BRSEL0	XPONRESET	SDIO1_PWR0	VSS	SDIO1_DAT0	SDIO1_DAT1	SDIO0_DAT1	SDIO0_DAT0	VSS	SDIO0_PWR0	VSS	FPD_DATP2	FPD_DATN1	FPD_CLKP	I2S_ECLK	I2S1_SDO	VSS	DDR_DQ63	VSS	XDDR_DQS7	DDR_DQ58	VSS	DDR_DQ50	2
1	VSS	HSSPI_CLK	HSSPI_DAT3	HSSPI_CSO0	ET_MDCLK	ET_RXCLK	ET_GTXCLK	VSS	EMMC_CLK	SCLKMAIN	EMMC_SDVCCQ	POFFCTL2	RTCLK	TMSEL0	BRSEL1	XSYSRESET	SDIO1_WP	SDIO1_CLK	SDIO1_CD	SDIO1_CMD	SDIO0_CMD	SDIO0_CD	SDIO0_CLK	SDIO0_WP	SCLK27M	VSS	FPD_DATP1	VSS	I2S_SCLK	VSS	SCLKDR3	DDR_DQ62	DDR_DQ60	DDR_DQS7	DDR_DQ59	DDR_DQ56	VSS	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	

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TopView

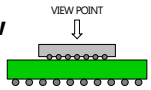


Figure 2-2: Ball assignment

2.3. Pin Information

The pin information is shown below.

2.3.1. Power Control

Table. 2-1: Power Control

Power Domain	Category	Signal name	I/O	Voltage[V]	VDDE	VDDI	Pullup /down	Comment
PD0	SYSTEM	POFFCTL[4:0]	O	1.8	VDEA	VDDA		

2.3.2. System Control

Table. 2-2: System Control

Power Domain	Category	Signal name	I/O	Voltage[V]	VDDE	VDDI	Pullup /down	Comment
PD1	SYSTEM	TCK	I	1.8	VDE	VDD_SCB	PU	JTAGTCK
		TMS	I/O	1.8	VDE	VDD_SCB	PU	JTAGTMS
		TDI	I	1.8	VDE	VDD_SCB	PU	TJAGTDI
		XTRST	I	1.8	VDE	VDD_SCB	PU	JTAGTRST
		TDO	O	1.8	VDE	VDD_SCB		JTAGTDO
		XSRST	I/O	1.8	VDE	VDD_SCB	PU	
		VPD[1:0]	I	0.9	VDD_SCB	VDD_SCB		For TEST(VSS)
		SCLKMAIN	I	1.8	VDE	VDD_SCB		CLK(25MHz)
		SCLKCA15	I	1.8	VDE	VDD_SCB		CLK(25MHz) for CA15
		SCLKCA7	I	1.8	VDE	VDD_SCB		CLK(25MHz) for CA7
(PD2)		SCLKDDR3	I	1.8	VDE2	VDD		CLK(33.33MHz)
(PD2)		SCLK27M	I	1.8	VDE2	VDD		CLK(27MHz) for FPD
(PD0)		RTCLK	I	1.8	VDEA	VDDA		CLK(32.768kHz)
(PD0)		XPONRESET	I	1.8	VDEA	VDDA	PU	PowerOnreset
		XSYSRESET	I	1.8	VDE	VDD_SCB	PU	SystemReset
		BRSEL[1:0]	I	1.8	VDE	VDD_SCB	PU	
(PD0)		DMS[1:0]	I	1.8	VDEA	VDDA	PD	DebugModeSelect (CM3DebugON)
		PCMODE[1:0]	I	1.8	VDE	VDD_SCB		Power control method selection
		PCMODE1	I	1.8	VDE	VDD_SCB	PD	0=I2C, 1=PONCTL
		PCMODE0	I	1.8	VDE	VDD_SCB	PU	0=LO, 1=HI
		TMSEL[6:0]	I	1.8	VDE	VDD_SCB	PD	For TEST(VSS)
(PD0)		WAKEUP	I	1.8	VDEA	VDDA	PD	For recovery from the Retention mode
(PD0)		TESTSEL	I	1.8	VDEA	VDDA	PD	

- VPD[1:0] should be kept fixed at 2'b00 during normal operation.
- FUSE_EN should be kept fixed at 1'b1 during normal operation.
- For details of BRSEL[1:0], refer to the BRSEL status register.
- For details of DMS, refer to the DMS of "Detailed specifications of Port MUX control function registers."
- TMSEL[6:0] should be kept fixed at 7'b0000000 during normal operation.
- TESTSEL should be kept fixed at 1'b0 during normal operation.

2.3.3. System Control Block

Table. 2-3: System Control Block

Power Domain	Category	Signal name	I/O	Voltage[V]	VDDE	VDDI	Pullup /down	Comment
PD1	SCB	PD[15:0]	I/O	1.8	VDE	VDD_SCB		GPIO
		PD15	I/O	1.8	VDE	VDD_SCB	PD	
		PD14	I/O	1.8	VDE	VDD_SCB	PD	
		PD13	I/O	1.8	VDE	VDD_SCB	PD	
		PD12	I/O	1.8	VDE	VDD_SCB	PD	
		PD11	I/O	1.8	VDE	VDD_SCB	PD	
		PD10	I/O	1.8	VDE	VDD_SCB	PD	
		PD9	I/O	1.8	VDE	VDD_SCB	PD	
		PD8	I/O	1.8	VDE	VDD_SCB	PD	
		PD7	I/O	1.8	VDE	VDD_SCB	PD	
		PD6	I/O	1.8	VDE	VDD_SCB	PD	
		PD5	I/O	1.8	VDE	VDD_SCB	PD	
		PD4	I/O	1.8	VDE	VDD_SCB	PD	
		PD3	I/O	1.8	VDE	VDD_SCB	PD	
		PD2	I/O	1.8	VDE	VDD_SCB	PD	
		PD1	I/O	1.8	VDE	VDD_SCB	PD	
		PD0	I/O	1.8	VDE	VDD_SCB	PD	
		PD[31:16]	I/O	1.8	VDE	VDD_SCB		GPIO
		PD31	I/O	1.8	VDE	VDD_SCB	PD	
		PD30	I/O	1.8	VDE	VDD_SCB	PD	
		PD29	I/O	1.8	VDE	VDD_SCB	PD	
		PD28	I/O	1.8	VDE	VDD_SCB	PD	
		PD27	I/O	1.8	VDE	VDD_SCB	PD	
		PD26	I/O	1.8	VDE	VDD_SCB	PD	
		PD25	I/O	1.8	VDE	VDD_SCB	PD	
		PD24	I/O	1.8	VDE	VDD_SCB	PD	
		PD23	I/O	1.8	VDE	VDD_SCB	PD	
		PD22	I/O	1.8	VDE	VDD_SCB	PD	
		PD21	I/O	1.8	VDE	VDD_SCB	PD	
		PD20	I/O	1.8	VDE	VDD_SCB	PD	
		PD19	I/O	1.8	VDE	VDD_SCB	PD	
		PD18	I/O	1.8	VDE	VDD_SCB	PD	
		PD17	I/O	1.8	VDE	VDD_SCB	PD	
		PD16	I/O	1.8	VDE	VDD_SCB	PD	
		PD[47:32]	I/O	1.8	VDE	VDD_SCB		GPIO
		PD47	I/O	1.8	VDE	VDD_SCB	PD	
		PD46	I/O	1.8	VDE	VDD_SCB	PD	
		PD45	I/O	1.8	VDE	VDD_SCB	PD	
		PD44	I/O	1.8	VDE	VDD_SCB	PD	
		PD43	I/O	1.8	VDE	VDD_SCB	PD	
		PD42	I/O	1.8	VDE	VDD_SCB	PD	
		PD41	I/O	1.8	VDE	VDD_SCB	PD	
		PD40	I/O	1.8	VDE	VDD_SCB	PD	
		PD39	I/O	1.8	VDE	VDD_SCB	PD	
		PD38	I/O	1.8	VDE	VDD_SCB	PD	
		PD37	I/O	1.8	VDE	VDD_SCB	PD	
		PD36	I/O	1.8	VDE	VDD_SCB	PD	
		PD35	I/O	1.8	VDE	VDD_SCB	PD	
		PD34	I/O	1.8	VDE	VDD_SCB	PD	
		PD33	I/O	1.8	VDE	VDD_SCB	PD	
		PD32	I/O	1.8	VDE	VDD_SCB	PD	
		PD[63:48]	I/O	1.8	VDE	VDD_SCB		GPIO
		PD63	I/O	1.8	VDE	VDD_SCB	PD	
		PD62	I/O	1.8	VDE	VDD_SCB	PD	
		PD61	I/O	1.8	VDE	VDD_SCB	PD	

Power Domain	Category	Signal name	I/O	Voltage[V]	VDDE	VDDI	Pullup /down	Comment
		PD60	I/O	1.8	VDE	VDD_SCB	PD	
		PD59	I/O	1.8	VDE	VDD_SCB	PD	
		PD58	I/O	1.8	VDE	VDD_SCB	PD	
		PD57	I/O	1.8	VDE	VDD_SCB	PD	
		PD56	I/O	1.8	VDE	VDD_SCB	PD	
		PD55	I/O	1.8	VDE	VDD_SCB	PD	
		PD54	I/O	1.8	VDE	VDD_SCB	PD	
		PD53	I/O	1.8	VDE	VDD_SCB	PD	
		PD52	I/O	1.8	VDE	VDD_SCB	PD	
		PD51	I/O	1.8	VDE	VDD_SCB	PD	
		PD50	I/O	1.8	VDE	VDD_SCB	PD	
		PD49	I/O	1.8	VDE	VDD_SCB	PD	
		PD48	I/O	1.8	VDE	VDD_SCB	PD	
		PD[65:64]	I/O	1.8	VDE	VDD_SCB		GPIO
		PD65	I/O	1.8	VDE	VDD_SCB	PD	
		PD64	I/O	1.8	VDE	VDD_SCB	PD	
	UARTch0	SIN0	I	1.8	VDE	VDD_SCB	PU	DSUB9pin#2RxD
		SOUT0	O	1.8	VDE	VDD_SCB		DSUB9pin#3TxD
		XCTS0	I	1.8	VDE	VDD_SCB	PU	DSUB9pin#8CTS
		XRTS0	O	1.8	VDE	VDD_SCB		DSUB9pin#7RTS
	I2Cch#0 forNon -secure	I2C0_SCL	I/O	1.8	VDE	VDD_SCB		I2CSCL
		I2C0_SDA	I/O	1.8	VDE	VDD_SCB		I2CSDA
	I2Cch#1 forNon -secure	I2C1_SCL	I/O	1.8	VDE	VDD_SCB		I2CSCL
		I2C1_SDA	I/O	1.8	VDE	VDD_SCB		I2CSDA
	I2Cch#7 forSecure	I2C2_SCL	I/O	1.8	VDE	VDD_SCB		I2CSCL
		I2C2_SDA	I/O	1.8	VDE	VDD_SCB		I2CSDA
	I2Cch#8 forSecure (Hs mode)	I2C3_SCL	I/O	1.8	VDE	VDD_SCB		I2CSCL
		I2C3_SDA	I/O	1.8	VDE	VDD_SCB		I2CSDA
	I2Cch#9 forSecure (Hs mode)	I2C4_SCL	I/O	1.8	VDE	VDD_SCB		I2CSCL
		I2C4_SDA	I/O	1.8	VDE	VDD_SCB		I2CSDA
	EtherMAC RGMIII/F	ET_GTXCLK	O	1.8	VDE	VDD_SCB		EtherGTXCLK
		ET_TXD[3:0]	O	1.8	VDE	VDD_SCB		EtherTXD
		ET_TXEN	O	1.8	VDE	VDD_SCB		EtherTXEN
		ET_RXCLK	I	1.8	VDE	VDD_SCB	PD	EtherRXCLK
		ET_RXD[3:0]	I	1.8	VDE	VDD_SCB		EtherRXD
		ET_RXDV	I	1.8	VDE	VDD_SCB		EtherRXDV
		ET_MDCLK	O	1.8	VDE	VDD_SCB		EtherMDCLK
		ET_MDIO	I/O	1.8	VDE	VDD_SCB		EtherMDIO
		ET_PME	I	1.8	VDE	VDD_SCB	PD	EtherPME
		ET_INT	I	1.8	VDE	VDD_SCB	PD	EtherINT
	HSSPI#0 (forBOOT#1)	HSSPI_CSO[1:0]	O	1.8	VDE	VDD_SCB		HSSPICSO
		HSSPI_CLK	I/O	1.8	VDE	VDD_SCB	PU	HSSPICLK
		HSSPI_DAT[3:0]	I/O	1.8	VDE	VDD_SCB	PU	HSSPIDAT
	eMMC	EMMC_CLK	O	1.8	VDE	VDD_SCB		eMMCCLK
		EMMC_CMD	I/O	1.8	VDE	VDD_SCB	PU	eMMCCMD
		EMMC_DAT[7:0]	I/O	1.8	VDE	VDD_SCB	PU	eMMCDAT
		EMMC_SDRSTN	O	1.8	VDE	VDD_SCB		eMMCSDRSTN
		EMMC_SDVCC	O	1.8	VDE	VDD_SCB		eMMCSDVCC
		EMMC_SDVCCQ	O	1.8	VDE	VDD_SCB		eMMCSDVCCQ

2.3.4. Media Processor Block

Table. 2-4: Media Processor Block

Power Domain	Category	Signal name	I/O	Voltage[V]	VDDE	VDDI	Pullup /down	Comment
PD2	PERIPHERAL I2S(F_SAIF) CLK+ch0-ch1	I2S_ECLK	I	1.8	VDE2	VDD	PD	I2SECLK
		I2S_SCLK	I/O	1.8	VDE2	VDD	PD	I2SSCLK
		I2S0_FSYN	I/O	1.8	VDE2	VDD	PD	I2SFSYN
		I2S0_SDO	I/O	1.8	VDE2	VDD	PD	I2SSDO
		I2S1_FSYN	I/O	1.8	VDE2	VDD	PD	I2SFSYN
		I2S1_SDO	I/O	1.8	VDE2	VDD	PD	I2SSDO
PD2	SDHOST#0 (MSIO)	SDIO0_CLK	O	3.3/1.8	VDE_SDIO0	VDD		SDIOCLK
		SDIO0_CMD	I/O	3.3/1.8	VDE_SDIO0	VDD		SDIOCMD
		SDIO0_DAT[3:0]	I/O	3.3/1.8	VDE_SDIO0	VDD		SDIODATA
		SDIO0_CD	I	1.8	VDE2	VDD	PU	SDIOCD
		SDIO0_WP	I	1.8	VDE2	VDD	PU	SDIOWP
		SDIO0_PWR0	O	1.8	VDE2	VDD		SDIOPWR0
		SDIO0_PWRERR	I	1.8	VDE2	VDD	PD	SDIOPWRERR
		SDIO0_VSEL	O	1.8	VDE2	VDD		SDIOVSEL
		VBIASP0	-	3.3/1.8	VDE_SDIO0	VDD		SDIOBIAS
		VBIASN0	-	3.3/1.8	VDE_SDIO0	VDD		SDIOBIAS
		VBIASPEXT0	-	3.3/1.8	VDE_SDIO0	VDD		SDIOBIAS
		VBIASNEXT0	-	3.3/1.8	VDE_SDIO0	VDD		SDIOBIAS
		VNODE_N0	-	3.3/1.8	VDE_SDIO0	VDD		SDIOBIAS
PD1	SDHOST#1 (MSIO)	SDIO1_CLK	O	3.3/1.8	VDE_SDIO1	VDD_SCB		SDIOCLK
		SDIO1_CMD	I/O	3.3/1.8	VDE_SDIO1	VDD_SCB		SDIOCMD
		SDIO1_DAT[3:0]	I/O	3.3/1.8	VDE_SDIO1	VDD_SCB		SDIODATA
		SDIO1_CD	I	1.8	VDE	VDD_SCB	PU	SDIOCD
		SDIO1_WP	I	1.8	VDE	VDD_SCB	PU	SDIOWP
		SDIO1_PWR0	O	1.8	VDE	VDD_SCB		SDIOPWR0
		SDIO1_PWRERR	I	1.8	VDE	VDD_SCB	PD	SDIOPWRERR
		SDIO1_VSEL	O	1.8	VDE	VDD_SCB		SDIOVSEL
		VBIASP1	-	3.3/1.8	VDE_SDIO1	VDD_SCB		SDIOBIAS
		VBIASN1	-	3.3/1.8	VDE_SDIO1	VDD_SCB		SDIOBIAS
		VBIASPEXT1	-	3.3/1.8	VDE_SDIO1	VDD_SCB		SDIOBIAS
		VBIASNEXT1	-	3.3/1.8	VDE_SDIO1	VDD_SCB		SDIOBIAS
		VNODE_N1	-	3.3/1.8	VDE_SDIO1	VDD_SCB		SDIOBIAS
PD17	FPDLinkTx	FPD_CLKP	O	1.8	VDE_FPD	VDD_FPD		FPDLinkClock(Posi)
		FPD_DATP[3:0]	O	1.8	VDE_FPD	VDD_FPD		FPDLinkDATA(Posi)
		FPD_CLKN	O	1.8	VDE_FPD	VDD_FPD		FPDLinkClock(Nega)
		FPD_DATN[3:0]	O	1.8	VDE_FPD	VDD_FPD		FPDLinkDATA(Nega)

2.3.5. Memory Block

Table. 2-5: Memory Block

Power Domain	Category	Signal name	I/O	Voltage[V]	VDDE	VDDI	Pullup /down	Comment
PD2	MEMORY	DDR_CLKO[3:0]	O	1.5/1.35	VDE15	VDD		DDRCLK(Posi)
		XDDR_CLKO[3:0]	O	1.5/1.35	VDE15	VDD		DDRCLK(Nega)
		DDR_ADD[15:0]	O	1.5/1.35	VDE15	VDD		DDRADDRESS
		DDR_BA[2:0]	O	1.5/1.35	VDE15	VDD		DDRBA
		XDDR_WE	O	1.5/1.35	VDE15	VDD		DDRWE
		XDDR_CAS	O	1.5/1.35	VDE15	VDD		DDRCAS
		XDDR_RAS	O	1.5/1.35	VDE15	VDD		DDRRAS
		XDDR_CS[3:0]	O	1.5/1.35	VDE15	VDD		DDRCS
(PD0)		DDR_CKE[3:0]	O	1.5/1.35	VDE15A	VDD		DDRCKE
(PD0)		XDDR_RESET	O	1.5/1.35	VDE15A	VDD		DDRRESET
		DDR_DQ[63:0]	I/O	1.5/1.35	VDE15	VDD		DDRDQ

Power Domain	Category	Signal name	I/O	Voltage[V]	VDDE	VDDI	Pullup /down	Comment
		DDR_DQM[7:0]	I/O	1.5/1.35	VDE15	VDD		DDRDQM
		DDR_DQS[7:0]	I/O	1.5/1.35	VDE15	VDD		DDRDQS(Posi)
		XDDR_DQS[7:0]	I/O	1.5/1.35	VDE15	VDD		DDRDQS(Nega)
		DDR_MZQRES	I/O	-	VDE15	VDD		DDRZQ
		DDR_MVREF	I	VDE15x0.5	VDE15	VDD		DDRVREF
		DDR_ODT[3:0]	O	1.5/1.35	VDE15	VDD		DDRODT
		DDR_DTO[1:0]	I/O	1.5/1.35	VDE15	VDD		DDRDTO
		DDR_ATO	O	1.5/1.35	VDE15	VDD		DDRATO

DDR_DTO[1:0], DDR_ATO should be set to Open during normal operation

2.3.6. High-speed I/O Block (PCIe)

Table. 2-6: High-speed I/O Block (PCIe)

Power Domain	Category	Signal name	I/O	Voltage[V]	VDDE	VDDI	Pullup /down	Comment
PD20	PCIe#0(HSIO)	PCIE0_REFCLKPI	I	0.9	VP_PCIE0	VP_PCIE0		PCIeCLK(Posi)
		PCIE0_REFCLKMI	I	0.9	VP_PCIE0	VP_PCIE0		PCIeCLK(Nega)
		PCIE0_REFRES_I	I	0.9	VP_PCIE0	VP_PCIE0		PCIeRESREF
		PCIE0_TXPO[3:0]	O	0.9	VPTX_PCIE0	VP_PCIE0		PCIeTx(Posi)
		PCIE0_TXNO[3:0]	O	0.9	VPTX_PCIE0	VP_PCIE0		PCIeTx(Nega)
		PCIE0_RXPI[3:0]	I	0.9	VP_PCIE0	VP_PCIE0		PCIeRx(Posi)
		PCIE0_RXNI[3:0]	I	0.9	VP_PCIE0	VP_PCIE0		PCIeRx(Nega)
(PD1)		PCIE0_PRVRETYPEI	I	1.8	VDE	VDD_SCB	PD	
(PD1)		XPCIE0_PERST	I/O	1.8	VDE	VDD_SCB	PD	
PD21	PCIe#1(HSIO)	PCIE1_REFCLKPI	I	0.9	VP_PCIE1	VP_PCIE1		PCIeCLK(Posi)
		PCIE1_REFCLKMI	I	0.9	VP_PCIE1	VP_PCIE1		PCIeCLK(Nega)
		PCIE1_REFRES_I	I	0.9	VP_PCIE1	VP_PCIE1		PCIeRESREF
		PCIE1_TXPO[3:0]	O	0.9	VPTX_PCIE1	VP_PCIE1		PCIeTx(Posi)
		PCIE1_TXNO[3:0]	O	0.9	VPTX_PCIE1	VP_PCIE1		PCIeTx(Nega)
		PCIE1_RXPI[3:0]	I	0.9	VP_PCIE1	VP_PCIE1		PCIeRx(Posi)
		PCIE1_RXNI[3:0]	I	0.9	VP_PCIE1	VP_PCIE1		PCIeRx(Nega)
(PD1)		PCIE1_X4_PRVRETYPEI	I	1.8	VDE	VDD_SCB	PD	Mode select for X4_LINK
(PD1)		XPCIE1_X4_PERST	I/O	1.8	VDE	VDD_SCB	PD	Reset for X4_LINK
(PD1)		PCIE1_X2_PRVRETYPEI	I	1.8	VDE	VDD_SCB	PD	Mode select for X2_LINK
(PD1)		XPCIE1_X2_PERST	I/O	1.8	VDE	VDD_SCB	PD	Reset for X2_LINK

2.3.7. High-speed I/O Block (USB)

Table. 2-7: High-speed I/O Block (USB)

Power Domain	Category	Signal name	I/O	Voltage[V]	VDDE	VDDI	Pullup /down	Comment
PD24	USB3.0HOST#0 (MSIO)	USB30_SSEARXIP	I	0.9	VDU_USB30	VDD_SCB		USB3.0SSRx(Posi)
		USB30_SSEARXIN	I	0.9	VDU_USB30	VDD_SCB		USB3.0SSRx(Nega)
		USB30_SSEXTXOP	O	0.9	VDN_USB30	VDD_SCB		USB3.0SSTx(Posi)
		USB30_SSEXTXON	O	0.9	VDN_USB30	VDD_SCB		USB3.0SSTx(Nega)
		USB30_HSDP	I/O	3.3	AVDF1_USB30	VDD_SCB		USB3.0HSD(Posi)
		USB30_HSDM	I/O	3.3	AVDF1_USB30	VDD_SCB		USB3.0HSD(Nega)
		USB30_HSEXT12K	O	-	AVDF1_USB30	VDD_SCB		USB3.0HSEXT12K(RES)
(PD1)		USB3_REFCLK	I	1.8	VDE	VDD_SCB	-	USB3.0REFCLK
(PD1)		USB30_VBUSCTRL	O	1.8	VDE	VDD_SCB		
(PD1)		USB30_OVERCRNT	I	1.8	VDE	VDD_SCB	PD	
PD25	USB3.0HOST#1 (MSIO)	USB31_SSEARXIP	I	0.9	VDU_USB31	VDD_SCB		USB3.0SSRx(Posi)
		USB31_SSEARXIN	I	0.9	VDU_USB31	VDD_SCB		USB3.0SSRx(Nega)
		USB31_SSEXTXOP	O	0.9	VDN_USB31	VDD_SCB		USB3.0SSTx(Posi)

Power Domain	Category	Signal name	I/O	Voltage[V]	VDDE	VDDI	Pullup /down	Comment
		USB31_SSEXTXON	O	0.9	VDN_USB31	VDD_SCB		USB3.0SSTx(Nega)
		USB31_HSDP	I/O	3.3	AVDF1_USB31	VDD_SCB		USB3.0HSD(Posi)
		USB31_HSDM	I/O	3.3	AVDF1_USB31	VDD_SCB		USB3.0HSD(Nega)
		USB31_HSEXT12K	O	-	AVDF1_USB31	VDD_SCB		USB3.0HSEXT12K(RES)
(PD1)		USB31_VBUSCTRL	O	1.8	VDE	VDD_SCB		
(PD1)		USB31_OVERCRNT	I	1.8	VDE	VDD_SCB	PD	
PD26	USB2.0HOST (MSIO)	USB2H_DP	I/O	3.3	AVDF1_USB2H	VDD_SCB		USB3.0HSD(Posi)
		USB2H_DM	I/O	3.3	AVDF1_USB2H	VDD_SCB		USB3.0HSD(Nega)
		USB2H_EXT12K	O	-	AVDF1_USB2H	VDD_SCB		USB3.0HSEXT12K(RES)
(PD1)		XUSB2H_OVCRNTI	I	1.8	VDE	VDD_SCB	PU	
(PD1)		USB2H_PRTPWRO	O	1.8	VDE	VDD_SCB		
PD27	USB2.0HOST /Device(MSIO)	USB2D_DP	I/O	3.3	AVDF1_USB2H DC	VDD_SCB		USB3.0HSD(Posi)
		USB2D_DM	I/O	3.3	AVDF1_USB2H DC	VDD_SCB		USB3.0HSD(Nega)
		USB2D_EXT12K	O	-	AVDF1_USB2H DC	VDD_SCB		USB3.0HSEXT12K(RES)
		XUSB2D_OVCRNTI	I	1.8	VDE	VDD_SCB	PU	
		USB2D_PRTPWRO	O	1.8	VDE	VDD_SCB		
		USB2D_VBUSVALI	I	1.8	VDE	VDD_SCB	PD	
		USB2D_IDDIGI	I	1.8	VDE	VDD_SCB		
		USB2D_DPUO	O	1.8	VDE	VDD_SCB		IDPullUP output

2.4. Initial Values for Pins

The initial values of MB86S72 pins when XPONRESET is applied are shown below.

2.4.1. Power Control

Table. 2-8: Power Control

Power Domain	Category	Signal name	I/O	Initial value	Comment
D0	SYSTEM	POFFCTL[4:0]	O		
		POFFCTL4	O	L	
		POFFCTL3	O	L	
		POFFCTL2	O	L	
		POFFCTL1	O	H	
		POFFCTL0	O	H	

2.4.2. System Control

Table. 2-9: System Control

Power Domain	Category	Signal name	I/O	Initial value	Comment
PD1	SYSTEM	TCK	I	—	
		TMS	I/O	INPUT	
		TDI	I	—	
		XTRST	I	—	
		TDO	O	L	
		XSRST	I/O	INPUT	"L" OUTPUT while applying Reset
		VPD[1:0]	I		
		VPD1	I	—	
		VPD0	I	—	
		SCLKMAIN	I	—	
		SCLKCA15	I	—	
		SCLKCA7	I	—	
(PD2)		SCLKDDR3	I	—	
(PD2)		SCLK27M	I	—	
(PD0)		RTCLK	I	—	
(PD0)		XPONRESET	I	—	
		XSYSRESET	I	—	
		BRSEL[1:0]	I		
		BRSEL1	I	—	
		BRSEL0	I	—	
(PD0)		DMS[1:0]	I		
		DMS1	I	—	
		DMS0	I	—	
		PCMODE[1:0]	I		
		PCMODE1	I	—	
		PCMODE0	I	—	
		TMSEL[6:0]	I		
		TMSEL6	I	—	
		TMSEL5	I	—	
		TMSEL4	I	—	
		TMSEL3	I	—	
		TMSEL2	I	—	
		TMSEL1	I	—	

Power Domain	Category	Signal name	I/O	Initial value	Comment
		TMSEL0	I	—	
(PD0)		WAKEUP	I	—	
(PD0)		TESTSEL	I	—	

2.4.3. System Control Block

Table. 2-10: System Control Block

Power Domain	Category	Signal name	I/O	Initial value	Comment
PD1	SCB	PD[15:0]	I/O		
		PD15	I/O	Hi-Z	
		PD14	I/O	Hi-Z	
		PD13	I/O	Hi-Z	
		PD12	I/O	Hi-Z	
		PD11	I/O	Hi-Z	
		PD10	I/O	Hi-Z	
		PD9	I/O	Hi-Z	
		PD8	I/O	Hi-Z	
		PD7	I/O	Hi-Z	
		PD6	I/O	Hi-Z	
		PD5	I/O	Hi-Z	
		PD4	I/O	Hi-Z	
		PD3	I/O	Hi-Z	
		PD2	I/O	Hi-Z	
		PD1	I/O	Hi-Z	
		PD0	I/O	Hi-Z	
		PD[31:16]	I/O		
		PD31	I/O	Hi-Z	
		PD30	I/O	Hi-Z	
		PD29	I/O	Hi-Z	
		PD28	I/O	Hi-Z	
		PD27	I/O	Hi-Z	
		PD26	I/O	Hi-Z	
		PD25	I/O	Hi-Z	
		PD24	I/O	Hi-Z	
		PD23	I/O	Hi-Z	
		PD22	I/O	Hi-Z	
		PD21	I/O	Hi-Z	
		PD20	I/O	Hi-Z	
		PD19	I/O	Hi-Z	
		PD18	I/O	Hi-Z	
		PD17	I/O	Hi-Z	
		PD16	I/O	Hi-Z	
		PD[47:32]	I/O		
		PD47	I/O	Hi-Z	
		PD46	I/O	Hi-Z	
		PD45	I/O	Hi-Z	
		PD44	I/O	Hi-Z	
		PD43	I/O	Hi-Z	
		PD42	I/O	Hi-Z	
		PD41	I/O	Hi-Z	
		PD40	I/O	Hi-Z	

Power Domain	Category	Signal name	I/O	Initial value	Comment
		PD39	I/O	Hi-Z	
		PD38	I/O	Hi-Z	
		PD37	I/O	Hi-Z	
		PD36	I/O	Hi-Z	
		PD35	I/O	Hi-Z	
		PD34	I/O	Hi-Z	
		PD33	I/O	Hi-Z	
		PD32	I/O	Hi-Z	
		PD[63:48]	I/O		
		PD63	I/O	Hi-Z	
		PD62	I/O	Hi-Z	
		PD61	I/O	Hi-Z	
		PD60	I/O	Hi-Z	
		PD59	I/O	Hi-Z	
		PD58	I/O	Hi-Z	
		PD57	I/O	Hi-Z	
		PD56	I/O	Hi-Z	
		PD55	I/O	Hi-Z	
		PD54	I/O	Hi-Z	
		PD53	I/O	Hi-Z	
		PD52	I/O	Hi-Z	
		PD51	I/O	Hi-Z	
		PD50	I/O	Hi-Z	
		PD49	I/O	Hi-Z	
		PD48	I/O	Hi-Z	
		PD[65:64]	I/O		
		PD65	I/O	Hi-Z	
		PD64	I/O	Hi-Z	
	UARTch0	SIN0	I	—	
		SOUT0	O	H	
		XCTS0	I	—	
		XRTS0	O	H	
	I2Cch#0 forNon-secure	I2C0_SCL	I/O	Hi-Z	
		I2C0_SDA	I/O	Hi-Z	
	I2Cch#1 forNon-secure	I2C1_SCL	I/O	Hi-Z	
		I2C1_SDA	I/O	Hi-Z	
	I2Cch#7 forSecure	I2C2_SCL	I/O	Hi-Z	
		I2C2_SDA	I/O	Hi-Z	
	I2Cch#8 forSecure (Hs mode)	I2C3_SCL	I/O	Hi-Z	
		I2C3_SDA	I/O	Hi-Z	
	I2Cch#9 forSecure (Hs mode)	I2C4_SCL	I/O	Hi-Z	
		I2C4_SDA	I/O	Hi-Z	
	EtherMAC RGMIII/F	ET_GTXCLK	O	H	
		ET_TXD[3:0]	O		
		ET_TXD3	O	L	
		ET_TXD2	O	L	
		ET_TXD1	O	L	
		ET_TXD0	O	L	
		ET_TXEN	O	L	
		ET_RXCLK	I	—	
		ET_RXD[3:0]	I		
		ET_RXD3	I	—	

Power Domain	Category	Signal name	I/O	Initial value	Comment
		ET_RXD2	I	—	
		ET_RXD1	I	—	
		ET_RXD0	I	—	
		ET_RXDV	I	—	
		ET_MDCLK	O	L	
		ET_MDIO	I/O	Hi-Z	
		ET_PME	I	—	
		ET_INT	I	—	
	HSSPI#0 (forBOOT#1)	HSSPI_CSO[1:0]	O		
		HSSPI_CSO1	O	Hi-Z	
		HSSPI_CSO0	O	Hi-Z	
		HSSPI_CLK	I/O	Hi-Z	
		HSSPI_DAT[3:0]	I/O		
		HSSPI_DAT3	I/O	Hi-Z	
		HSSPI_DAT2	I/O	Hi-Z	
		HSSPI_DAT1	I/O	Hi-Z	
		HSSPI_DAT0	I/O	Hi-Z	
	eMMC	EMMC_CLK	O	L	
		EMMC_CMD	I/O	H	
		EMMC_DAT[7:0]	I/O		
		EMMC_DAT7	I/O	H	
		EMMC_DAT6	I/O	H	
		EMMC_DAT5	I/O	H	
		EMMC_DAT4	I/O	H	
		EMMC_DAT3	I/O	H	
		EMMC_DAT2	I/O	H	
		EMMC_DAT1	I/O	H	
		EMMC_DAT0	I/O	H	
		EMMC_SDRSTN	O	L	
		EMMC_SDVCC	O	L	
		EMMC_SDVCCQ	O	L	

2.4.4. Media Processor Block

Table. 2-11: Media Processor Block

Power Domain	Category	Signal name	I/O	Initial value	Comment
PD2	PERIPHERAL I2S(F_SAIF) CLK+ch0-ch1	I2S_ECLK	I	—	
		I2S_SCLK	I/O	Hi-Z	
		I2S0_FSYN	I/O	Hi-Z	
		I2S0_SDO	I/O	Hi-Z	
		I2S1_FSYN	I/O	Hi-Z	
		I2S1_SDO	I/O	Hi-Z	
PD2	SDHOST#0 (MSIO)	SDIO0_CLK	O	L	
		SDIO0_CMD	I/O	H	
		SDIO0_DAT[3:0]	I/O		
		SDIO0_DAT3	I/O	H	
		SDIO0_DAT2	I/O	H	
		SDIO0_DAT1	I/O	H	
		SDIO0_DAT0	I/O	H	
		SDIO0_CD	I	—	
		SDIO0_WP	I	—	
		SDIO0_PWR0	O	L	

Power Domain	Category	Signal name	I/O	Initial value	Comment
		SDIO0_PWRERR	I	—	
		SDIO0_VSEL	O	L	
		VBIASP0	-	—	
		VBIASN0	-	—	
		VBIASPEXT0	-	—	
		VBIASNEXT0	-	—	
		VNODE_N0	-	—	
PD1	SDHOST#1 (MSIO)	SDIO1_CLK	O	L	
		SDIO1_CMD	I/O	H	
		SDIO1_DAT[3:0]	I/O		
		SDIO1_DAT3	I/O	H	
		SDIO1_DAT2	I/O	H	
		SDIO1_DAT1	I/O	H	
		SDIO1_DAT0	I/O	H	
		SDIO1_CD	I	—	
		SDIO1_WP	I	—	
		SDIO1_PWR0	O	L	
		SDIO1_PWRERR	I	—	
		SDIO1_VSEL	O	L	
		VBIASP1	-	—	
		VBIASN1	-	—	
		VBIASPEXT1	-	—	
		VBIASNEXT1	-	—	
		VNODE_N1	-	—	
PD17	FPDLinkTx	FPD_CLKP	O	L	
		FPD_DATP[3:0]	O		
		FPD_DATP3	O	L	
		FPD_DATP2	O	L	
		FPD_DATP1	O	L	
		FPD_DATP0	O	L	
		FPD_CLKN	O	H	
		FPD_DATN[3:0]	O		
		FPD_DATN3	O	H	
		FPD_DATN2	O	H	
		FPD_DATN1	O	H	
		FPD_DATN0	O	H	

2.4.5. Memory Block

Table. 2-12: Memory Block

Power Domain	Category	Signal name	I/O	Initial value	Comment
PD2	MEMORY	DDR_CLKO[3:0]	O		
		DDR_CLKO3	O	L	
		DDR_CLKO2	O	L	
		DDR_CLKO1	O	L	
		DDR_CLKO0	O	L	
		XDDR_CLKO[3:0]	O		
		XDDR_CLKO3	O	H	
		XDDR_CLKO2	O	H	
		XDDR_CLKO1	O	H	
		XDDR_CLKO0	O	H	
		DDR_ADD[15:0]	O		

Power Domain	Category	Signal name	I/O	Initial value	Comment
		DDR_ADD15	O	L	
		DDR_ADD14	O	L	
		DDR_ADD13	O	L	
		DDR_ADD12	O	L	
		DDR_ADD11	O	L	
		DDR_ADD10	O	L	
		DDR_ADD9	O	L	
		DDR_ADD8	O	L	
		DDR_ADD7	O	L	
		DDR_ADD6	O	L	
		DDR_ADD5	O	L	
		DDR_ADD4	O	L	
		DDR_ADD3	O	L	
		DDR_ADD2	O	L	
		DDR_ADD1	O	L	
		DDR_ADD0	O	L	
		DDR_BA[2:0]	O		
		DDR_BA2	O	L	
		DDR_BA1	O	L	
		DDR_BA0	O	L	
		XDDR_WE	O	L	
		XDDR_CAS	O	L	
		XDDR_RAS	O	H	
		XDDR_CS[3:0]	O		
		XDDR_CS3	O	H	
		XDDR_CS2	O	H	
		XDDR_CS1	O	H	
		XDDR_CS0	O	H	
(PD0)		DDR_CKE[3:0]	O		
		DDR_CKE3	O	L	
		DDR_CKE2	O	L	
		DDR_CKE1	O	L	
		DDR_CKE0	O	L	
(PD0)		XDDR_RESET	O	L	
		DDR_DQ[63:0]	I/O		
		DDR_DQ63	I/O	Hi-Z	
		DDR_DQ62	I/O	Hi-Z	
		DDR_DQ61	I/O	Hi-Z	
		DDR_DQ60	I/O	Hi-Z	
		DDR_DQ59	I/O	Hi-Z	
		DDR_DQ58	I/O	Hi-Z	
		DDR_DQ57	I/O	Hi-Z	
		DDR_DQ56	I/O	Hi-Z	
		DDR_DQ55	I/O	Hi-Z	
		DDR_DQ54	I/O	Hi-Z	
		DDR_DQ53	I/O	Hi-Z	
		DDR_DQ52	I/O	Hi-Z	
		DDR_DQ51	I/O	Hi-Z	
		DDR_DQ50	I/O	Hi-Z	
		DDR_DQ49	I/O	Hi-Z	
		DDR_DQ48	I/O	Hi-Z	
		DDR_DQ47	I/O	Hi-Z	
		DDR_DQ46	I/O	Hi-Z	

Power Domain	Category	Signal name	I/O	Initial value	Comment
		DDR_DQ45	I/O	Hi-Z	
		DDR_DQ44	I/O	Hi-Z	
		DDR_DQ43	I/O	Hi-Z	
		DDR_DQ42	I/O	Hi-Z	
		DDR_DQ41	I/O	Hi-Z	
		DDR_DQ40	I/O	Hi-Z	
		DDR_DQ39	I/O	Hi-Z	
		DDR_DQ38	I/O	Hi-Z	
		DDR_DQ37	I/O	Hi-Z	
		DDR_DQ36	I/O	Hi-Z	
		DDR_DQ35	I/O	Hi-Z	
		DDR_DQ34	I/O	Hi-Z	
		DDR_DQ33	I/O	Hi-Z	
		DDR_DQ32	I/O	Hi-Z	
		DDR_DQ31	I/O	Hi-Z	
		DDR_DQ30	I/O	Hi-Z	
		DDR_DQ29	I/O	Hi-Z	
		DDR_DQ28	I/O	Hi-Z	
		DDR_DQ27	I/O	Hi-Z	
		DDR_DQ26	I/O	Hi-Z	
		DDR_DQ25	I/O	Hi-Z	
		DDR_DQ24	I/O	Hi-Z	
		DDR_DQ23	I/O	Hi-Z	
		DDR_DQ22	I/O	Hi-Z	
		DDR_DQ21	I/O	Hi-Z	
		DDR_DQ20	I/O	Hi-Z	
		DDR_DQ19	I/O	Hi-Z	
		DDR_DQ18	I/O	Hi-Z	
		DDR_DQ17	I/O	Hi-Z	
		DDR_DQ16	I/O	Hi-Z	
		DDR_DQ15	I/O	Hi-Z	
		DDR_DQ14	I/O	Hi-Z	
		DDR_DQ13	I/O	Hi-Z	
		DDR_DQ12	I/O	Hi-Z	
		DDR_DQ11	I/O	Hi-Z	
		DDR_DQ10	I/O	Hi-Z	
		DDR_DQ9	I/O	Hi-Z	
		DDR_DQ8	I/O	Hi-Z	
		DDR_DQ7	I/O	Hi-Z	
		DDR_DQ6	I/O	Hi-Z	
		DDR_DQ5	I/O	Hi-Z	
		DDR_DQ4	I/O	Hi-Z	
		DDR_DQ3	I/O	Hi-Z	
		DDR_DQ2	I/O	Hi-Z	
		DDR_DQ1	I/O	Hi-Z	
		DDR_DQ0	I/O	Hi-Z	
		DDR_DQM[7:0]	I/O		
		DDR_DQM7	I/O	Hi-Z	
		DDR_DQM6	I/O	Hi-Z	
		DDR_DQM5	I/O	Hi-Z	
		DDR_DQM4	I/O	Hi-Z	
		DDR_DQM3	I/O	Hi-Z	
		DDR_DQM2	I/O	Hi-Z	

Power Domain	Category	Signal name	I/O	Initial value	Comment
		DDR_DQM1	I/O	Hi-Z	
		DDR_DQM0	I/O	Hi-Z	
		DDR_DQS[7:0]	I/O		
		DDR_DQS7	I/O	Hi-Z	
		DDR_DQS6	I/O	Hi-Z	
		DDR_DQS5	I/O	Hi-Z	
		DDR_DQS4	I/O	Hi-Z	
		DDR_DQS3	I/O	Hi-Z	
		DDR_DQS2	I/O	Hi-Z	
		DDR_DQS1	I/O	Hi-Z	
		DDR_DQS0	I/O	Hi-Z	
		XDDR_DQS[7:0]	I/O		
		XDDR_DQS7	I/O	Hi-Z	
		XDDR_DQS6	I/O	Hi-Z	
		XDDR_DQS5	I/O	Hi-Z	
		XDDR_DQS4	I/O	Hi-Z	
		XDDR_DQS3	I/O	Hi-Z	
		XDDR_DQS2	I/O	Hi-Z	
		XDDR_DQS1	I/O	Hi-Z	
		XDDR_DQS0	I/O	Hi-Z	
		DDR_MZQRES	I/O	Hi-Z	
		DDR_MVREF	I	—	
		DDR_ODT[3:0]	O		
		DDR_ODT3	O	L	
		DDR_ODT2	O	L	
		DDR_ODT1	O	L	
		DDR_ODT0	O	L	
		DDR_DTO[1:0]	I/O		
		DDR_DTO1	I/O	Hi-Z	
		DDR_DTO0	I/O	Hi-Z	
		DDR_ATO	O	Hi-Z	

2.4.6. High-speed I/O Block (PCIe)

Table. 2-13: High-speed I/O Block (PCIe)

Power Domain	Category	Signal name	I/O	Initial value	Comment
PD20	PCIe#0(HSIO)	PCIE0_REFCLKPI	I	—	
		PCIE0_REFCLKMI	I	—	
		PCIE0_REFRES_I	I	—	
		PCIE0_TXPO[3:0]	O		
		PCIE0_TXPO3	O	Hi-Z	
		PCIE0_TXPO2	O	Hi-Z	
		PCIE0_TXPO1	O	Hi-Z	
		PCIE0_TXPO0	O	Hi-Z	
		PCIE0_TXNO[3:0]	O		
		PCIE0_TXNO3	O	Hi-Z	
		PCIE0_TXNO2	O	Hi-Z	
		PCIE0_TXNO1	O	Hi-Z	
		PCIE0_TXNO0	O	Hi-Z	
		PCIE0_RXPI[3:0]	I		

Power Domain	Category	Signal name	I/O	Initial value	Comment
		PCIE0_RXPI3	I	—	
		PCIE0_RXPI2	I	—	
		PCIE0_RXPI1	I	—	
		PCIE0_RXPI0	I	—	
		PCIE0_RXNI[3:0]	I		
		PCIE0_RXNI3	I	—	
		PCIE0_RXNI2	I	—	
		PCIE0_RXNI1	I	—	
		PCIE0_RXNI0	I	—	
(PD1)		PCIE0_PRVRETYPEI	I	—	
(PD1)		XPCIE0_PERST	I/O	INPUT	
PD21	PCIe#1(HSIO)	PCIE1_REFCLKPI	I	—	
		PCIE1_REFCLKMI	I	—	
		PCIE1_REFRES_I	I	—	
		PCIE1_TXPO[3:0]	O		
		PCIE1_TXPO3	O	Hi-Z	
		PCIE1_TXPO2	O	Hi-Z	
		PCIE1_TXPO1	O	Hi-Z	
		PCIE1_TXPO0	O	Hi-Z	
		PCIE1_TXNO[3:0]	O		
		PCIE1_TXNO3	O	Hi-Z	
		PCIE1_TXNO2	O	Hi-Z	
		PCIE1_TXNO1	O	Hi-Z	
		PCIE1_TXNO0	O	Hi-Z	
		PCIE1_RXPI[3:0]	I		
		PCIE1_RXPI3	I	—	
		PCIE1_RXPI2	I	—	
		PCIE1_RXPI1	I	—	
		PCIE1_RXPI0	I	—	
		PCIE1_RXNI[3:0]	I		
		PCIE1_RXNI3	I	—	
		PCIE1_RXNI2	I	—	
		PCIE1_RXNI1	I	—	
		PCIE1_RXNI0	I	—	
(PD1)		PCIE1_X4_PRVRETYPEI	I	—	
(PD1)		XPCIE1_X4_PERST	I/O	INPUT	
(PD1)		PCIE1_X2_PRVRETYPEI	I	—	
(PD1)		XPCIE1_X2_PERST	I/O	INPUT	

2.4.7. High-speed I/O Block (USB)

Table. 2-14: High-speed I/O Block (USB)

Power Domain	Category	Signal name	I/O	Initial value	Comment
PD24	USB3.0HOST#0 (MSIO)	USB30_SSEARXIP	I	—	
		USB30_SSEARXIN	I	—	
		USB30_SSEXTXOP	O	Hi-Z	
		USB30_SSEXTXON	O	Hi-Z	
		USB30_HSDP	I/O	Hi-Z	
		USB30_HSDM	I/O	Hi-Z	
		USB30_HSEXT12K	O	—	resistance
(PD1)		USB3_REFCLK	I	—	
(PD1)		USB30_VBUSCTRL	O	L	
(PD1)		USB30_OVERCRNT	I	—	
PD25	USB3.0HOST#1 (MSIO)	USB31_SSEARXIP	I	—	
		USB31_SSEARXIN	I	—	
		USB31_SSEXTXOP	O	Hi-Z	
		USB31_SSEXTXON	O	Hi-Z	
		USB31_HSDP	I/O	Hi-Z	
		USB31_HSDM	I/O	Hi-Z	
		USB31_HSEXT12K	O	—	resistance
(PD1)		USB31_VBUSCTRL	O	L	
(PD1)		USB31_OVERCRNT	I	—	
PD26	USB2.0HOST (MSIO)	USB2H_DP	I/O	Hi-Z	
		USB2H_DM	I/O	Hi-Z	
		USB2H_EXT12K	O	—	resistance
(PD1)		XUSB2H_OVCRNTI	I	—	
(PD1)		USB2H_PRTPWRO	O	L	
PD27	USB2.0HOST /Device(MSIO)	USB2D_DP	I/O	Hi-Z	
		USB2D_DM	I/O	Hi-Z	
		USB2D_EXT12K	O	—	resistance
		XUSB2D_OVCRNTI	I	—	
		USB2D_PRTPWRO	O	L	
		USB2D_VBUSVALI	I	—	
		USB2D_IDDIGI	I	—	
		USB2D_DPUO	O	L	

2.5. Power Supply Specifications

Some of the macros installed in this SoC require analog power supplies in addition to the digital power supply. In the PCB, it is necessary that the supply of power to the analog circuits is done separated from the supply of power to the digital circuits. In addition, an analog power supply must be provided only to an individual macro that requires it.

2.5.1. List of Digital Power Supplies

Table 2-15: Digital power supply

Macro name	Power supply PIN	Voltage [V]	Description
IO cell	VDEA	1.800	VDE (Power down mode)
	VDE	1.800	Fail Safe IO VDE
	VDE2	1.800	Fail Safe IO VDE2
	VDE15A	1.500 / 1.350	SSTL15 VDE (Power down mode)
	VDE15	1.500 / 1.350	SSTL15 VDE
FPDLink	VDE_FPD	1.800	FPDLink VDE
SDIO#0	VDE_SDIO0	1.800 / 3.300 *1	SDIO VDE
SDIO#1	VDE_SDIO1	1.800 / 3.300 *1	SDIO VDE
Logic core	VDDA	0.900	Core VDD (Power down mode)
	VDD	0.900	Core VDD
	VDD_SCB	0.900	SCB VDD
Cortex-A7	VDD_CA7	0.900 - 1.010	CA7 VDD
Cortex-A15	VDD_CA15	0.900 - 1.010	CA15 VDD
FPDLink	VDD_FPD	0.900	FPDLink VDD

*1: Do not use SDIO#0 and SDIO#1 simultaneously at 3.3V.

2.5.2. List of Analog Power Supplies

Table 2-16: Analog power supply

Macro name	Power supply PIN	Voltage	Description
PLL	AVD_PLL[8:7,5:1]	0.900	PLL VDD
DDR PLL	VAA_PLL1/2	1.800	PLL VDD for DDR-PHY
PCIe	VPTX_PCIE1/0	0.900	PCIe VPTX0
	VPH_PCIE1/0	1.800	PCIe VPH
	VP_PCIE1/0	0.900	PCIe VP
USB3.0	VDU_USB31/30	0.900	USB3.0 VDU
	VDN_USB31/30	0.900	USB3.0 VDN
	AVDF1_USB31/30	3.300	USB3.0 AVDF1
	AVDF2_USB31/30	0.900	USB3.0 AVDF2
	AVDP_USB31/30	0.900	USB3.0 AVDP
	AVD18_USB31/30	1.800	USB3.0 AVD18
USB2.0	AVDF1_USB2H/HDC	3.300	USB2.0 AVDF1
	AVDF2_USB2H/HDC	0.900	USB2.0 AVDF2
	AVDP_USB2H/HDC	0.900	USB2.0 AVDP
	AVD18_USB2H/HDC	1.800	USB2.0 AVD18
Temperature Sensor	AVDH_CA15_0	1.800	Temperature Sensor AVDH for CA15 CPU0
	AVDH_CA15_1	1.800	Temperature Sensor AVDH for CA15 CPU1
	AVDH_CA7_0	1.800	Temperature Sensor AVDH for CA7 CPU0
	AVDH_CA7_1	1.800	Temperature Sensor AVDH for CA7 CPU1
	AVDH_DDR	1.800	Temperature Sensor AVDH for DDRC
	AVDH_MALI	1.800	Temperature Sensor AVDH for Mali

2.6. Pin Sharing

In MB86S72, PD (Port Data) signals (PD0-PD65) share pins with other signals. The details of this pin sharing are given below.

2.6.1. Pin Sharing Configuration

The pin sharing connection block diagram is shown below. For details of the sharing PD signal and the peripheral signal, see Section 2.6.2 List of Shared Pins.

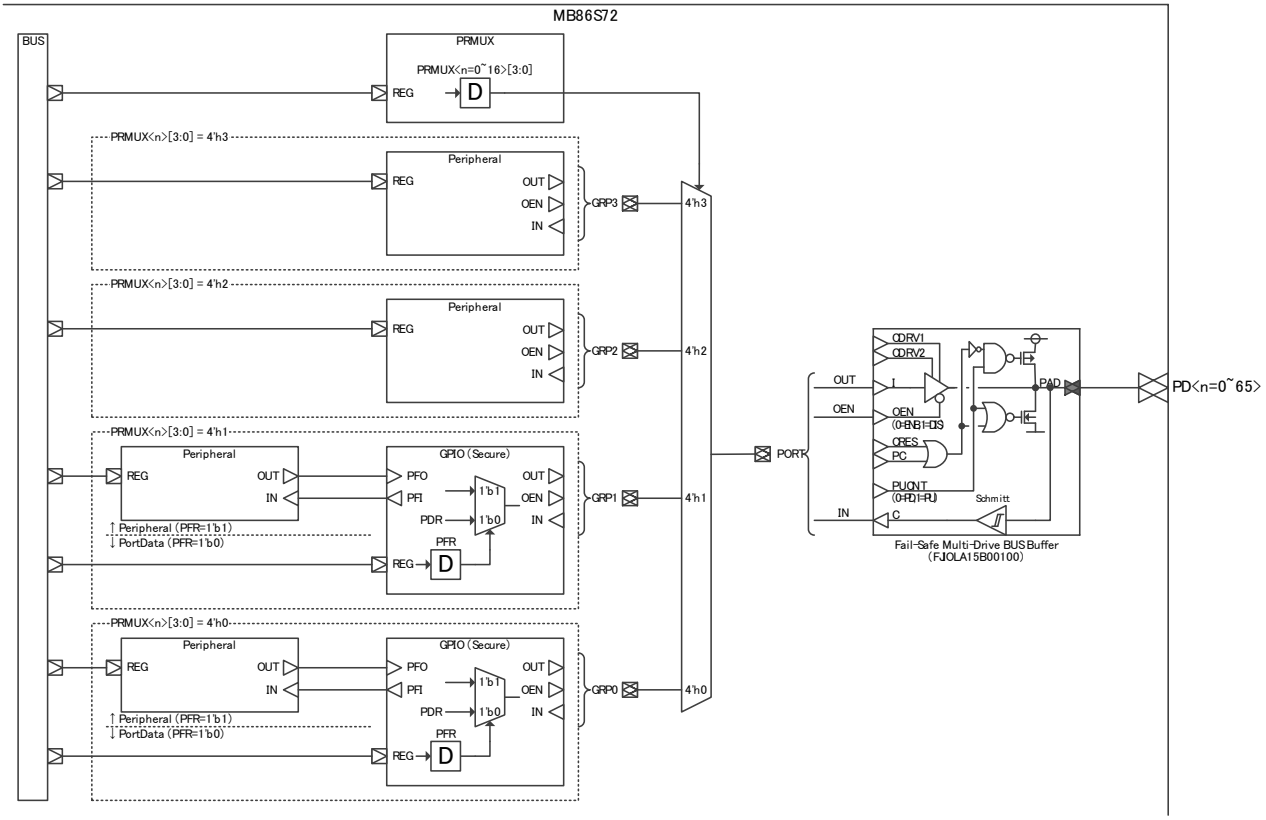


Figure 2-3: Pin sharing block diagram

2.6.2. List of Shared Pins

In MB86S72, selection of the functions of the shared pins is done by assigning any function to each selection group (4 pins).
The part of the list of pins which has an orange colored background indicate the initial selection pin functions immediately after a reset.
In the case of group 0 and group 1, the function changes depending on the function selection state of the power supply control pin (PCMODE[1]). When used as a power supply control pin, PD0 to PD6 cannot be used as a general purpose pin because it is being used dedicatedly for the power supply control function.

The following table has been color coded as follows.

Content of selection immediately after RESET (PRMUX[n])
Content of selection immediately after RESET (GPIO)
Explicit selection group is necessary (GPIO)
PONCTL (for only power supply)
No connection

2.6.2.1. PRMUX register 3'h0

The pins present in each pin sharing Function Group#0 are described in this section.

PRMUX<Selection group>=3'h0

Table 2-17: PRMUX<Selection group>=3'h0

	PRMUX register set value			3'h0					
	Selection Group	DTK assignment	Pin location	Group	Direction	Name	Group	Direction	Name
			PFR[n]	1'b0 (GPIO Mode)			1'b1 (Peripheral Mode)		
When PCMODE[1]=1'b1 (using power supply control pins)	0	PONCTL0 (for only power supply)	PD0	PMU			PONCTL0 (for PCIe#0)		
		PONCTL1 (for only power supply)	PD1				PONCTL1 (for PCIe#1)		
		PONCTL2 (for only power supply)	PD2				PONCTL2 (for USB3.0 HOST#0)		
		PONCTL3 (for only power supply)	PD3				PONCTL3 (for USB3.0 HOST#1)		
	1	PONCTL4 (for only power supply)	PD4				PONCTL4 (for USB2.0 HOST)		
		PONCTL5 (for only power supply)	PD5				PONCTL5 (for USB2.0 HOST/Device)		
		PONCTL6 (for only power supply)	PD6				PONCTL6 (for Display Macro)		
		GPIO Extend / EXINT31	PD7	GPIO#0 (for SCB)	BD(IN)	PDR0[7]		IN	(No connection)
When PCMODE[1]=1'b0 (USING GPIO)	0	GPIO Extend / EXINT24	PD0	GPIO#0 (for SCB) SCB=0xF3040000, AP =(access denied)	BD(IN)	PDR0[0]		IN	(No connection)
		GPIO Extend / EXINT25	PD1		BD(IN)	PDR0[1]		IN	(No connection)
		GPIO Extend / EXINT26	PD2		BD(IN)	PDR0[2]		IN	(No connection)
		GPIO Extend / EXINT27	PD3		BD(IN)	PDR0[3]		IN	(No connection)
	1	GPIO Extend / EXINT28	PD4		BD(IN)	PDR0[4]		IN	(No connection)
		GPIO Extend / EXINT29	PD5		BD(IN)	PDR0[5]		IN	(No connection)
		GPIO Extend / EXINT30	PD6		BD(IN)	PDR0[6]		IN	(No connection)
		GPIO Extend / EXINT31	PD7		BD(IN)	PDR0[7]		IN	(No connection)

	PRMUX register set value			3'h0					
	Selection Group	DTK assignment	Pin location	Group	Direction	Name	Group	Direction	Name
			PFR[n]	1'b0 (GPIO Mode)			1'b1 (Peripheral Mode)		
PCMODE SHARED	2	S/W Reset (ETHER PHY)	PD8		BD(IN)	PDR1[0]		IN	(No connection)
		S/W Power On Reset	PD9		BD(IN)	PDR1[1]		IN	(No connection)
		GPIO Extend	PD10		BD(IN)	PDR1[2]		IN	(No connection)
		GPIO Extend	PD11		BD(IN)	PDR1[3]		IN	(No connection)
	3	GPIO Extend	PD12		BD(IN)	PDR1[4]		IN	(No connection)
		GPIO Extend	PD13		BD(IN)	PDR1[5]		IN	(No connection)
		GPIO Extend	PD14		BD(IN)	PDR1[6]		IN	(No connection)
		GPIO Extend	PD15		BD(IN)	PDR1[7]		IN	(No connection)
	4	UART#1 (DCD1)	PD16		BD(IN)	PDR2[0]		IN	(No connection)
		UART#1 (RXD1)	PD17		BD(IN)	PDR2[1]		IN	(No connection)
		UART#1 (TXD1)	PD18		BD(IN)	PDR2[2]		IN	(No connection)
		UART#1 (DTR1)	PD19		BD(IN)	PDR2[3]		IN	(No connection)
	5	UART#1 (DSR1)	PD20		BD(IN)	PDR2[4]		IN	(No connection)
		UART#1 (RTS1)	PD21		BD(IN)	PDR2[5]		IN	(No connection)
		UART#1 (CTS1)	PD22		BD(IN)	PDR2[6]		IN	(No connection)
		UART#1 (RI1)	PD23		BD(IN)	PDR2[7]		IN	(No connection)
	6	GPIO Extend	PD24		BD(IN)	PDR3[0]		IN	(No connection)
		GPIO Extend	PD25		BD(IN)	PDR3[1]		IN	(No connection)
		GPIO Extend	PD26		BD(IN)	PDR3[2]		IN	(No connection)
		GPIO Extend	PD27		BD(IN)	PDR3[3]		IN	(No connection)
	7	GPIO Extend / general purpose DIP-SW	PD28		BD(IN)	PDR3[4]		IN	(No connection)
		GPIO Extend / general purpose DIP-SW	PD29		BD(IN)	PDR3[5]		IN	(No connection)
		GPIO Extend / general purpose DIP-SW	PD30		BD(IN)	PDR3[6]		IN	(No connection)
		GPIO Extend / general purpose DIP-SW	PD31		BD(IN)	PDR3[7]		IN	(No connection)
	8	GPIO Extend / EXINT0	PD32		IN	(No connection)			
		GPIO Extend / EXINT1	PD33		IN	(No connection)			
		GPIO Extend / EXINT2	PD34		IN	(No connection)			
		GPIO Extend / EXINT3	PD35		IN	(No connection)			
	9	HOME KEY	PD36		IN	(No connection)			
		POWER KEY	PD37		IN	(No connection)			
		UP KEY	PD38		IN	(No connection)			
		DOWN KEY	PD39		IN	(No connection)			
	10	EXINT8 (PCIe#0 PRSNT2#)	PD40		IN	(No connection)			
		EXINT9 (PCIe#1 PRSNT2#)	PD41		IN	(No connection)			
		EXINT10 (LCD PANEL)	PD42		IN	(No connection)			
		EXINT11 (RTC INTRA)	PD43		IN	(No connection)			

	PRMUX register set value			3'h0					
	Selection Group	DTK assignment	Pin location	Group	Direction	Name	Group	Direction	Name
			PFR[n]	1'b0 (GPIO Mode)			1'b1 (Peripheral Mode)		
	11	GPIO Extend / EXINT12 (TRACE)	PD44		IN	(No connection)			
		GPIO Extend / EXINT13 (TRACE)	PD45		IN	(No connection)			
		GPIO Extend / EXINT14 (TRACE)	PD46		IN	(No connection)			
		GPIO Extend / EXINT15 (TRACE)	PD47		IN	(No connection)			
	12	GPIO Extend / EXINT16 (TRACE)	PD48		IN	(No connection)			
		GPIO Extend / EXINT17 (TRACE)	PD49		IN	(No connection)			
		GPIO Extend / EXINT18 (TRACE)	PD50		IN	(No connection)			
		GPIO Extend / EXINT19 (TRACE)	PD51		IN	(No connection)			
	13	GPIO Extend / EXINT20 (TRACE)	PD52		IN	(No connection)			
		GPIO Extend / EXINT21 (TRACE)	PD53		IN	(No connection)			
		GPIO Extend / EXINT22 (TRACE)	PD54		IN	(No connection)			
		GPIO Extend / EXINT23 (TRACE)	PD55		IN	(No connection)			
	14	GPIO Extend / CFG0 (TRACE)	PD56		IN	(No connection)			
		GPIO Extend / CFG1 (TRACE)	PD57		IN	(No connection)			
		GPIO Extend / CFG2 (TRACE)	PD58		IN	(No connection)			
		GPIO Extend / CFG3 (TRACE)	PD59		IN	(No connection)			
	15	GPIO Extend / CFG4 (TRACE)	PD60		IN	(No connection)			
		GPIO Extend / CFG5 (TRACE)	PD61		IN	(No connection)			
		GPIO Extend / CFG6 (LED-green)	PD62		IN	(No connection)			
		GPIO Extend / CFG7(LED-red)	PD63		IN	(No connection)			
	16	BOOT MODE SEL	PD64	BRSEL	IN	BRSEL2			
		BOOT MODE SEL	PD65		IN	BRSEL3			

2.6.2.2. PRMUX register 3'h1

The pins present in each pin sharing Function Group#1 are described in this section.

Table 2-18: PRMUX<Selection group>=3'h1

	PRMUX register set value			3'h1					
	Selection Group	DTK assignment	Pin location	Group	Direction	Name	Group	Direction	Name
			PFR[n]	1'b0 (GPIO Mode)			1'b1 (Peripheral Mode)		
When PCMODE[1]=1'b1 (using power supply control pins)	0	PONCTL0 (for only power supply)	PD0	PMU	PONCTL0 (for PCIe#0)				
		PONCTL1 (for only power supply)	PD1		PONCTL1 (for PCIe#1)				
		PONCTL2 (for only power supply)	PD2		PONCTL2 (for USB3.0 HOST#0)				
		PONCTL3 (for only power supply)	PD3		PONCTL3 (for USB3.0 HOST#1)				
	1	PONCTL4 (for only power supply)	PD4		PONCTL4 (for USB2.0 HOST)				
		PONCTL5 (for only power supply)	PD5		PONCTL5 (for USB2.0 HOST/Device)				
		PONCTL6 (for only power supply)	PD6		PONCTL6 (for Display Macro)				
		GPIO Extend / EXINT31	PD7	GPIO#1 (for AP)	BD(IN)	PDR0[7]	EXIU	OUT	EXINT31
When PCMODE[1]=1'b0 (USING GPIO)	0	GPIO Extend / EXINT24	PD0	GPIO#1 (for AP) SCB=0xD1000000, AP=0x0031000000	BD(IN)	PDR0[0]	EXIU AP=0x00310C0000	OUT	EXINT24
		GPIO Extend / EXINT25	PD1		BD(IN)	PDR0[1]		OUT	EXINT25
		GPIO Extend / EXINT26	PD2		BD(IN)	PDR0[2]		OUT	EXINT26
		GPIO Extend / EXINT27	PD3		BD(IN)	PDR0[3]		OUT	EXINT27
	1	GPIO Extend / EXINT28	PD4		BD(IN)	PDR0[4]		OUT	EXINT28
		GPIO Extend / EXINT29	PD5		BD(IN)	PDR0[5]		OUT	EXINT29
		GPIO Extend / EXINT30	PD6		BD(IN)	PDR0[6]		OUT	EXINT30
		GPIO Extend / EXINT31	PD7		BD(IN)	PDR0[7]		OUT	EXINT31
PCMODE SHARED	2	S/W Reset (ETHER PHY)	PD8		BD(IN)	PDR1[0]	UART#0 AP=0x0031040000	IN	DCD0
		S/W Power On Reset	PD9		BD(IN)	PDR1[1]		IN	(Not used)
		GPIO Extend	PD10		BD(IN)	PDR1[2]		OUT	(Not used)
		GPIO Extend	PD11		BD(IN)	PDR1[3]		OUT	DTR0
	3	GPIO Extend	PD12		BD(IN)	PDR1[4]		IN	DSR0
		GPIO Extend	PD13		BD(IN)	PDR1[5]		OUT	(Not used)
		GPIO Extend	PD14		BD(IN)	PDR1[6]		IN	(Not used)
		GPIO Extend	PD15		BD(IN)	PDR1[7]		IN	RI0
	4	UART#1 (DCD1)	PD16		BD(IN)	PDR2[0]	UART#1 AP=0x0031050000	IN	DCD1
		UART#1 (RXD1)	PD17		BD(IN)	PDR2[1]		IN	RXD1
		UART#1 (TXD1)	PD18		BD(IN)	PDR2[2]		OUT	TXD1
		UART#1 (DTR1)	PD19		BD(IN)	PDR2[3]		OUT	DTR1
	5	UART#1 (DSR1)	PD20		BD(IN)	PDR2[4]		IN	DSR1
		UART#1 (RTS1)	PD21		BD(IN)	PDR2[5]		OUT	RTS1
		UART#1 (CTS1)	PD22		BD(IN)	PDR2[6]		IN	CTS1

	PRMUX register set value			3'h1					
	Selection Group	DTK assignment	Pin location	Group	Direction	Name	Group	Direction	Name
			PFR[n]	1'b0 (GPIO Mode)			1'b1 (Peripheral Mode)		
		UART#1 (RI1)	PD23	GPIO#2 (for AP) SCB=0xD1010000, AP=0x0031010000	BD(IN)	PDR2[7]		IN	RI1
	6	GPIO Extend	PD24		BD(IN)	PDR3[0]	UART#2 AP=0x0031060000	IN	DCD2
		GPIO Extend	PD25		BD(IN)	PDR3[1]		IN	RXD2
		GPIO Extend	PD26		BD(IN)	PDR3[2]		OUT	TXD2
		GPIO Extend	PD27		BD(IN)	PDR3[3]		OUT	DTR2
	7	GPIO Extend / general purpose DIP-SW	PD28		BD(IN)	PDR3[4]		IN	DSR2
		GPIO Extend / general purpose DIP-SW	PD29		BD(IN)	PDR3[5]		OUT	RTS2
		GPIO Extend / general purpose DIP-SW	PD30		BD(IN)	PDR3[6]		IN	CTS2
		GPIO Extend / general purpose DIP-SW	PD31		BD(IN)	PDR3[7]		IN	RI2
	8	GPIO Extend / EXINT0	PD32		BD(IN)	PDR0[0]	EXIU AP=0x00310C0000	IN	EXINT0
		GPIO Extend / EXINT1	PD33		BD(IN)	PDR0[1]		IN	EXINT1
		GPIO Extend / EXINT2	PD34		BD(IN)	PDR0[2]		IN	EXINT2
		GPIO Extend / EXINT3	PD35		BD(IN)	PDR0[3]		IN	EXINT3
	9	HOME KEY	PD36		BD(IN)	PDR0[4]		IN	EXINT4
		POWER KEY	PD37		BD(IN)	PDR0[5]		IN	EXINT5
		UP KEY	PD38		BD(IN)	PDR0[6]		IN	EXINT6
		DOWN KEY	PD39		BD(IN)	PDR0[7]		IN	EXINT7
	10	EXINT8 (PCIe#0 PRSNT2#)	PD40		BD(IN)	PDR1[0]		IN	EXINT8
		EXINT9 (PCIe#1 PRSNT2#)	PD41		BD(IN)	PDR1[1]		IN	EXINT9
		EXINT10 (LCD PANEL)	PD42		BD(IN)	PDR1[2]		IN	EXINT10
		EXINT11 (RTC INTRA)	PD43		BD(IN)	PDR1[3]		IN	EXINT11
	11	GPIO Extend / EXINT12 (TRACE)	PD44		BD(IN)	PDR1[4]		IN	EXINT12
		GPIO Extend / EXINT13 (TRACE)	PD45		BD(IN)	PDR1[5]		IN	EXINT13
		GPIO Extend / EXINT14 (TRACE)	PD46		BD(IN)	PDR1[6]		IN	EXINT14
		GPIO Extend / EXINT15 (TRACE)	PD47		BD(IN)	PDR1[7]		IN	EXINT15
	12	GPIO Extend / EXINT16 (TRACE)	PD48		BD(IN)	PDR2[0]		IN	EXINT16
		GPIO Extend / EXINT17 (TRACE)	PD49		BD(IN)	PDR2[1]		IN	EXINT17
		GPIO Extend / EXINT18 (TRACE)	PD50		BD(IN)	PDR2[2]		IN	EXINT18
		GPIO Extend / EXINT19 (TRACE)	PD51		BD(IN)	PDR2[3]		IN	EXINT19
	13	GPIO Extend / EXINT20 (TRACE)	PD52		BD(IN)	PDR2[4]		IN	EXINT20
		GPIO Extend / EXINT21 (TRACE)	PD53		BD(IN)	PDR2[5]		IN	EXINT21
		GPIO Extend / EXINT22 (TRACE)	PD54		BD(IN)	PDR2[6]		IN	EXINT22
		GPIO Extend / EXINT23 (TRACE)	PD55		BD(IN)	PDR2[7]		IN	EXINT23
	14	GPIO Extend / CFG0 (TRACE)	PD56		BD(IN)	PDR3[0]	Configuration (MRBC) AP=0x00310F0000	IN	CFG0
		GPIO Extend / CFG1 (TRACE)	PD57		BD(IN)	PDR3[1]		IN	CFG1
		GPIO Extend / CFG2 (TRACE)	PD58		BD(IN)	PDR3[2]		IN	CFG2
		GPIO Extend / CFG3 (TRACE)	PD59		BD(IN)	PDR3[3]		IN	CFG3
	15	GPIO Extend / CFG4 (TRACE)	PD60		BD(IN)	PDR3[4]		IN	CFG4

	PRMUX register set value			3'h1					
	Selection Group	DTK assignment	Pin location	Group	Direction	Name	Group	Direction	Name
			PFR[n]	1'b0 (GPIO Mode)			1'b1 (Peripheral Mode)		
		GPIO Extend / CFG5 (TRACE)	PD61		BD(IN)	PDR3[5]		IN	CFG5
		GPIO Extend / CFG6 (LED-green)	PD62		BD(IN)	PDR3[6]		IN	CFG6
		GPIO Extend / CFG7(LED-red)	PD63		BD(IN)	PDR3[7]		IN	CFG7
	16	BOOT MODE SEL	PD64		IN	(No connection)			
		BOOT MODE SEL	PD65		IN	(No connection)			

2.6.2.2.1 UART#0 (Extended control signals)

This group represents the control signals of UART#0. Dedicated pins are present for data communication and flow control signals.

Table. 2-19: UART#0 I/F

PD	Pin	Direction	Sync	Polarity	Initial value	Connection destination	Function description
8	PD8/DCD0	I	---		---		Data Carrier Detect
9	PD9						
10	PD10						
11	PD11/DTR0	O	---		1'b1		Data Transmit Ready
12	PD12/DSR0	I	---		---		Data Set Ready
13	PD13						
14	PD14						
15	PD15/RI0	I	---		---		Ring Indicator

2.6.2.2.2 UART#1

This group represents the signals of UART#1.

Table. 2-20: UART#1 I/F

PD	Pin	Direction	Sync	Polarity	Initial value	Connection destination	Function description
16	PD16/DCD1	I	---		---	UART#1	Data Carrier Detect
17	PD17/RXD1	I	---		---	UART#1	Receive Data
18	PD18/TXD1	O	---		1'b1	UART#1	Transmit Data
19	PD19/DTR1	O	---		1'b1	UART#1	Data Transmit Ready
20	PD20/DSR1	I	---		---	UART#1	Data Set Ready
21	PD21/RTS1	O	---		1'b1	UART#1	Transmit Request
22	PD22/CTS1	I	---		---	UART#1	Transmit Clear
23	PD23/RI1	I	---		---	UART#1	Ring Indicator

2.6.2.2.3 UART#2

This group represents the signals of UART#2.

Table. 2-21: UART#2 I/F

PD	Pin	Direction	Sync	Polarity	Initial value	Connection destination	Function description
24	PD24/DCD2	I	---		---	UART#2	Data Carrier Detect
25	PD25/RXD2	I	---		---	UART#2	Receive Data
26	PD26/TXD2	O	---		1'b1	UART#2	Transmit Data
27	PD27/DTR2	O	---		1'b1	UART#2	Data Transmit Ready
28	PD28/DSR2	I	---		---	UART#2	Data Set Ready
29	PD29/RTS2	O	---		1'b1	UART#2	Transmit Request
30	PD30/CTS2	I	---		---	UART#2	Transmit Clear
31	PD31/RI2	I	---		---	UART#2	Ring Indicator

2.6.2.2.4 External interrupts

This group represents the signals of external interrupts.

Table 2-22: External interrupts

PD	Pin	Direction	Sync	Polarity	Initial value	Connection destination	Function description
32	PD32/EXINT0	I	---		---	EXIU	External Interrupt
33	PD33/EXINT1	I	---		---	EXIU	External Interrupt
34	PD34/EXINT2	I	---		---	EXIU	External Interrupt
35	PD35/EXINT3	I	---		---	EXIU	External Interrupt
36	PD36/EXINT4	I	---		---	EXIU	External Interrupt
37	PD37/EXINT5	I	---		---	EXIU	External Interrupt
38	PD38/EXINT6	I	---		---	EXIU	External Interrupt
39	PD39/EXINT7	I	---		---	EXIU	External Interrupt
40	PD40/EXINT8	I	---		---	EXIU	External Interrupt
41	PD41/EXINT9	I	---		---	EXIU	External Interrupt
42	PD42/EXINT10	I	---		---	EXIU	External Interrupt
43	PD43/EXINT11	I	---		---	EXIU	External Interrupt
44	PD44/EXINT12	I	---		---	EXIU	External Interrupt
45	PD45/EXINT13	I	---		---	EXIU	External Interrupt
46	PD46/EXINT14	I	---		---	EXIU	External Interrupt
47	PD47/EXINT15	I	---		---	EXIU	External Interrupt
48	PD48/EXINT16	I	---		---	EXIU	External Interrupt
49	PD49/EXINT17	I	---		---	EXIU	External Interrupt
50	PD50/EXINT18	I	---		---	EXIU	External Interrupt
51	PD51/EXINT19	I	---		---	EXIU	External Interrupt
52	PD52/EXINT20	I	---		---	EXIU	External Interrupt
53	PD53/EXINT21	I	---		---	EXIU	External Interrupt
54	PD54/EXINT22	I	---		---	EXIU	External Interrupt
55	PD55/EXINT23	I	---		---	EXIU	External Interrupt

2.6.2.2.5 Pin Config

This group represents the signals of pin configuration.

Table 2-23: External pin configuration

PD	Pin	Direction	Sync	Polarity	Initial value	Connection destination	Function description
56	PD56/CFG0	I	---		---	MRBC	
57	PD57/CFG1	I	---		---	MRBC	
58	PD58/CFG2	I	---		---	MRBC	
59	PD59/CFG3	I	---		---	MRBC	
60	PD60/CFG4	I	---		---	MRBC	
61	PD61/CFG5	I	---		---	MRBC	
62	PD62/CFG6	I	---		---	MRBC	
63	PD63/CFG7	I	---		---	MRBC	

2.6.2.3. PRMUX register 3'h2

The pins present in each pin sharing Function Group#2 are described in this section.

Table 2-24: PRMUX<Selection group>=3'h2

	PRMUX register set value			3'h2		
	Selection Group	DTK assignment	Pin location	Group	Direction	Name
			PFR[n]	---		
When PCMODE[1]=1'b1 (using power supply control pins)	0	PONCTL0 (for only power supply)	PD0	PMU	PONCTL0 (for PCIe#0)	
		PONCTL1 (for only power supply)	PD1		PONCTL1 (for PCIe#1)	
		PONCTL2 (for only power supply)	PD2		PONCTL2 (for USB3.0 HOST#0)	
		PONCTL3 (for only power supply)	PD3		PONCTL3 (for USB3.0 HOST#1)	
	1	PONCTL4 (for only power supply)	PD4		PONCTL4 (for USB2.0 HOST)	
		PONCTL5 (for only power supply)	PD5		PONCTL5 (for USB2.0 HOST/Device)	
		PONCTL6 (for only power supply)	PD6		PONCTL6 (for Display Macro)	
		GPIO Extend / EXINT31	PD7		IN	(No connection)
When PCMODE[1]=1'b0 (USING GPIO)	0	GPIO Extend / EXINT24	PD0		IN	(No connection)
		GPIO Extend / EXINT25	PD1		IN	(No connection)
		GPIO Extend / EXINT26	PD2		IN	(No connection)
		GPIO Extend / EXINT27	PD3		IN	(No connection)
	1	GPIO Extend / EXINT28	PD4		IN	(No connection)
		GPIO Extend / EXINT29	PD5		IN	(No connection)
		GPIO Extend / EXINT30	PD6		IN	(No connection)
		GPIO Extend / EXINT31	PD7		IN	(No connection)
PCMODE SHARED	2	S/W Reset (ETHER PHY)	PD8	NAND Controller SCB=0xF2200000, AP=(access denied)	BD(IN)	D0
		S/W Power On Reset	PD9		BD(IN)	D1
		GPIO Extend	PD10		BD(IN)	D2
		GPIO Extend	PD11		BD(IN)	D3
	3	GPIO Extend	PD12		BD(IN)	D4
		GPIO Extend	PD13		BD(IN)	D5
		GPIO Extend	PD14		BD(IN)	D6
		GPIO Extend	PD15		BD(IN)	D7
	4	UART#1 (DCD1)	PD16		BD(IN)	D8
		UART#1 (RXD1)	PD17		BD(IN)	D9
		UART#1 (TXD1)	PD18		BD(IN)	D10
		UART#1 (DTR1)	PD19		BD(IN)	D11
	5	UART#1 (DSR1)	PD20		BD(IN)	D12
		UART#1 (RTS1)	PD21		BD(IN)	D13
		UART#1 (CTS1)	PD22		BD(IN)	D14
		UART#1 (RI1)	PD23		BD(IN)	D15
	6	GPIO Extend	PD24		OUT	CS0
		GPIO Extend	PD25		OUT	CS1
		GPIO Extend	PD26		IN	BUSY
		GPIO Extend	PD27		OUT	ALE

	PRMUX register set value			3'h2		
	Selection Group	DTK assignment	Pin location	Group	Direction	Name
			PFR[n]	---		
	7	GPIO Extend / general purpose DIP-SW	PD28		OUT	CLE
		GPIO Extend / general purpose DIP-SW	PD29		OUT	WE
		GPIO Extend / general purpose DIP-SW	PD30		OUT	RE
		GPIO Extend / general purpose DIP-SW	PD31		IN	(No connection)
	8	GPIO Extend / EXINT0	PD32		IN	(No connection)
		GPIO Extend / EXINT1	PD33		IN	(No connection)
		GPIO Extend / EXINT2	PD34		IN	(No connection)
		GPIO Extend / EXINT3	PD35		IN	(No connection)
	9	HOME KEY	PD36		IN	(No connection)
		POWER KEY	PD37		IN	(No connection)
		UP KEY	PD38		IN	(No connection)
		DOWN KEY	PD39		IN	(No connection)
	10	EXINT8 (PCIe#0 PRSNT2#)	PD40		IN	(No connection)
		EXINT9 (PCIe#1 PRSNT2#)	PD41		IN	(No connection)
		EXINT10 (LCD PANEL)	PD42		IN	(No connection)
		EXINT11 (RTC INTRA)	PD43		IN	(No connection)
	11	GPIO Extend / EXINT12 (TRACE)	PD44	TRACE AP=0x0020010000	OUT	DATA0
		GPIO Extend / EXINT13 (TRACE)	PD45		OUT	DATA1
		GPIO Extend / EXINT14 (TRACE)	PD46		OUT	DATA2
		GPIO Extend / EXINT15 (TRACE)	PD47		OUT	DATA3
	12	GPIO Extend / EXINT16 (TRACE)	PD48		OUT	DATA4
		GPIO Extend / EXINT17 (TRACE)	PD49		OUT	DATA5
		GPIO Extend / EXINT18 (TRACE)	PD50		OUT	DATA6
		GPIO Extend / EXINT19 (TRACE)	PD51		OUT	DATA7
	13	GPIO Extend / EXINT20 (TRACE)	PD52		OUT	DATA8
		GPIO Extend / EXINT21 (TRACE)	PD53		OUT	DATA9
		GPIO Extend / EXINT22 (TRACE)	PD54		OUT	DATA10
		GPIO Extend / EXINT23 (TRACE)	PD55		OUT	DATA11
	14	GPIO Extend / CFG0 (TRACE)	PD56		OUT	DATA12
		GPIO Extend / CFG1 (TRACE)	PD57		OUT	DATA13
		GPIO Extend / CFG2 (TRACE)	PD58		OUT	DATA14
		GPIO Extend / CFG3 (TRACE)	PD59		OUT	DATA15
	15	GPIO Extend / CFG4 (TRACE)	PD60		OUT	CLK
		GPIO Extend / CFG5 (TRACE)	PD61		OUT	CTL
		GPIO Extend / CFG6 (LED-green)	PD62		IN	(No connection)
		GPIO Extend / CFG7(LED-red)	PD63		IN	(No connection)
	16	BOOT MODE SEL	PD64		IN	(No connection)
		BOOT MODE SEL	PD65		IN	(No connection)

2.6.2.3.1 NAND

This group represents the signals of the NAND I/F.

Table. 2-25: NAND I/F

PD	Pin	Direction	Sync	Polarity	Initial value	Connection destination	Function description
8	NANDD0	I/O	---		---	PL244	Data0
9	NANDD1	I/O	---		---	PL244	Data1
10	NANDD2	I/O	---		---	PL244	Data2
11	NANDD3	I/O	---		---	PL244	Data3
12	NANDD4	I/O	---		---	PL244	Data4
13	NANDD5	I/O	---		---	PL244	Data5
14	NANDD6	I/O	---		---	PL244	Data6
15	NANDD7	I/O	---		---	PL244	Data7
16	NANDD8	I/O	---		---	PL244	Data8
17	NANDD9	I/O	---		---	PL244	Data9
18	NANDD10	I/O	---		---	PL244	Data10
19	NANDD11	I/O	---		---	PL244	Data11
20	NANDD12	I/O	---		---	PL244	Data12
21	NANDD13	I/O	---		---	PL244	Data13
22	NANDD14	I/O	---		---	PL244	Data14
23	NANDD15	I/O	---		---	PL244	Data15
24	NANDCS0	O	---		1'b0	PL244	ChipSelect#0
25	NANDCS1	O	---		1'b0	PL244	ChipSelect#1
26	NANDBUSY	I	---		---	PL244	BusySignal
27	NANDALE	O	---		1'b0	PL244	AddressLatch
28	NANDCLE	O	---		1'b0	PL244	CycleLatch
29	NANDWE	O	---		1'b0	PL244	WriteEnable
30	NANDRE	O	---		1'b0	PL244	ReadEnable

2.6.2.3.2 TRACE

This group represents the signals of TRACE I/F

Table. 2-26: TRACE I/F

PD	Pin	Direction	Sync	Polarity	Initial value	Connection destination	Function description
44	TRACEDATA0	O	TRACECLK		1'b0	CSSYS	Trace Data0
45	TRACEDATA1	O	TRACECLK		1'b0	CSSYS	Trace Data1
46	TRACEDATA2	O	TRACECLK		1'b0	CSSYS	Trace Data2
47	TRACEDATA3	O	TRACECLK		1'b0	CSSYS	Trace Data3
48	TRACEDATA4	O	TRACECLK		1'b0	CSSYS	Trace Data4
49	TRACEDATA5	O	TRACECLK		1'b0	CSSYS	Trace Data5
50	TRACEDATA6	O	TRACECLK		1'b0	CSSYS	Trace Data6
51	TRACEDATA7	O	TRACECLK		1'b0	CSSYS	Trace Data7
52	TRACEDATA8	O	TRACECLK		1'b0	CSSYS	Trace Data8
53	TRACEDATA9	O	TRACECLK		1'b0	CSSYS	Trace Data9
54	TRACEDATA10	O	TRACECLK		1'b0	CSSYS	Trace Data10
55	TRACEDATA11	O	TRACECLK		1'b0	CSSYS	Trace Data11
56	TRACEDATA12	O	TRACECLK		1'b0	CSSYS	Trace Data12
57	TRACEDATA13	O	TRACECLK		1'b0	CSSYS	Trace Data13
58	TRACEDATA14	O	TRACECLK		1'b0	CSSYS	Trace Data14
59	TRACEDATA15	O	TRACECLK		1'b0	CSSYS	Trace Data15
60	TRACECLK	O	---		1'b0	CSSYS	Trace Clock
61	TRACECTL	O	TRACECLK		1'b0	CSSYS	Trace Control

2.6.2.4. PRMUX register 3'h3

The pins present in each pin sharing Function Group#3 are described in this section.

Table 2-27: PRMUX<Selection group>=3'h3

	PRMUX register set value			3'h3		
	Selection Group	DTK assignment	Pin location	Group	Direction	Name
			PFR[n]	---		
When PCMODE[1]=1'b1 (using power supply control pins)	0	PONCTL0 (for only power supply)	PD0	PMU	PONCTL0 (for PCIe#0)	
		PONCTL1 (for only power supply)	PD1		PONCTL1 (for PCIe#1)	
		PONCTL2 (for only power supply)	PD2		PONCTL2 (for USB3.0 HOST#0)	
		PONCTL3 (for only power supply)	PD3		PONCTL3 (for USB3.0 HOST#1)	
	1	PONCTL4 (for only power supply)	PD4		PONCTL4 (for USB2.0 HOST)	
		PONCTL5 (for only power supply)	PD5		PONCTL5 (for USB2.0 HOST/Device)	
		PONCTL6 (for only power supply)	PD6		PONCTL6 (for Display Macro)	
		GPIO Extend / EXINT31	PD7		IN	(No connection)
When PCMODE[1]=1'b0 (USING GPIO)	0	GPIO Extend / EXINT24	PD0		IN	(No connection)
		GPIO Extend / EXINT25	PD1		IN	(No connection)
		GPIO Extend / EXINT26	PD2		IN	(No connection)
		GPIO Extend / EXINT27	PD3		IN	(No connection)
	1	GPIO Extend / EXINT28	PD4		IN	(No connection)
		GPIO Extend / EXINT29	PD5		IN	(No connection)
		GPIO Extend / EXINT30	PD6		IN	(No connection)
		GPIO Extend / EXINT31	PD7		IN	(No connection)
PCMODE SHARED	2	S/W Reset (ETHER PHY)	PD8	Static Memory Controller (MEMCS) SCB=0xF2320000, AP=(access denied)	OUT	XCS0 (CS[3])
		S/W Power On Reset	PD9		OUT	XCS1 (CS[4])
		GPIO Extend	PD10		OUT	XRD
		GPIO Extend	PD11		OUT	XWR0
	3	GPIO Extend	PD12		OUT	XWR1
		GPIO Extend	PD13		OUT	XWE
		GPIO Extend	PD14		BD(IN)	ED0
		GPIO Extend	PD15		BD(IN)	ED1
	4	UART#1 (DCD1)	PD16		BD(IN)	ED2
		UART#1 (RXD1)	PD17		BD(IN)	ED3
		UART#1 (TXD1)	PD18		BD(IN)	ED4
		UART#1 (DTR1)	PD19		BD(IN)	ED5
	5	UART#1 (DSR1)	PD20		BD(IN)	ED6
		UART#1 (RTS1)	PD21		BD(IN)	ED7
		UART#1 (CTS1)	PD22		BD(IN)	ED8
		UART#1 (RI1)	PD23		BD(IN)	ED9
	6	GPIO Extend	PD24		BD(IN)	ED10
		GPIO Extend	PD25		BD(IN)	ED11
		GPIO Extend	PD26		BD(IN)	ED12
		GPIO Extend	PD27		BD(IN)	ED13

	PRMUX register set value			3'h3		
	Selection Group	DTK assignment	Pin location	Group	Direction	Name
			PFR[n]	---		
	7	GPIO Extend / general purpose DIP-SW	PD28		BD(IN)	ED14
		GPIO Extend / general purpose DIP-SW	PD29		BD(IN)	ED15
		GPIO Extend / general purpose DIP-SW	PD30		IN	RDY
		GPIO Extend / general purpose DIP-SW	PD31		OUT	EA0
	8	GPIO Extend / EXINT0	PD32		OUT	EA1
		GPIO Extend / EXINT1	PD33		OUT	EA2
		GPIO Extend / EXINT2	PD34		OUT	EA3
		GPIO Extend / EXINT3	PD35		OUT	EA4
	9	HOME KEY	PD36		OUT	EA5
		POWER KEY	PD37		OUT	EA6
		UP KEY	PD38		OUT	EA7
		DOWN KEY	PD39		OUT	EA8
	10	EXINT8 (PCIe#0 PRSNT2#)	PD40		OUT	EA9
		EXINT9 (PCIe#1 PRSNT2#)	PD41		OUT	EA10
		EXINT10 (LCD PANEL)	PD42		OUT	EA11
		EXINT11 (RTC INTRA)	PD43		OUT	EA12
	11	GPIO Extend / EXINT12 (TRACE)	PD44		OUT	EA13
		GPIO Extend / EXINT13 (TRACE)	PD45		OUT	EA14
		GPIO Extend / EXINT14 (TRACE)	PD46		OUT	EA15
		GPIO Extend / EXINT15 (TRACE)	PD47		OUT	EA16
	12	GPIO Extend / EXINT16 (TRACE)	PD48		OUT	EA17
		GPIO Extend / EXINT17 (TRACE)	PD49		OUT	EA18
		GPIO Extend / EXINT18 (TRACE)	PD50		OUT	EA19
		GPIO Extend / EXINT19 (TRACE)	PD51		OUT	EA20
	13	GPIO Extend / EXINT20 (TRACE)	PD52		OUT	EA21
		GPIO Extend / EXINT21 (TRACE)	PD53		OUT	EA22
		GPIO Extend / EXINT22 (TRACE)	PD54		OUT	EA23
		GPIO Extend / EXINT23 (TRACE)	PD55		OUT	EA24
	14	GPIO Extend / CFG0 (TRACE)	PD56		OUT	(Not used)
		GPIO Extend / CFG1 (TRACE)	PD57		OUT	(Not used)
		GPIO Extend / CFG2 (TRACE)	PD58		OUT	(Not used)
		GPIO Extend / CFG3 (TRACE)	PD59		OUT	(Not used)
	15	GPIO Extend / CFG4 (TRACE)	PD60		OUT	(Not used)
		GPIO Extend / CFG5 (TRACE)	PD61		OUT	(Not used)
		GPIO Extend / CFG6 (LED-green)	PD62		IN	(No connection)
		GPIO Extend / CFG7(LED-red)	PD63		IN	(No connection)
	16	BOOT MODE SEL	PD64		IN	(No connection)
		BOOT MODE SEL	PD65		IN	(No connection)

2.6.2.4.1 Static Memory Controller

This group represents the signals of Static Memory Controller I/F.

Table. 2-28: Static Memory Controller I/F

PD	Pin	Direction	Sync	Polarity	Initial value	Connection destination	Function description
8	XCS0	O	---		1'b1	MEMCS	Chip Select[0]
9	XCS1	O	---		1'b1	MEMCS	Chip Select[1]
10	XRD	O	---		1'b1	MEMCS	Read Enable
11	XWR0	O	---		1'b1	MEMCS	Write Enable0
12	XWR1	O	---		1'b1	MEMCS	Write Enable1
13	XWE	O	---		1'b1	MEMCS	Write Enable
14	ED0	I/O	---		---	MEMCS	Data0
15	ED1	I/O	---		---	MEMCS	Data1
16	ED2	I/O	---		---	MEMCS	Data2
17	ED3	I/O	---		---	MEMCS	Data3
18	ED4	I/O	---		---	MEMCS	Data4
19	ED5	I/O	---		---	MEMCS	Data5
20	ED6	I/O	---		---	MEMCS	Data6
21	ED7	I/O	---		---	MEMCS	Data7
22	ED8	I/O	---		---	MEMCS	Data8
23	ED9	I/O	---		---	MEMCS	Data9
24	ED10	I/O	---		---	MEMCS	Data10
25	ED11	I/O	---		---	MEMCS	Data11
26	ED12	I/O	---		---	MEMCS	Data12
27	ED13	I/O	---		---	MEMCS	Data13
28	ED14	I/O	---		---	MEMCS	Data14
29	ED15	I/O	---		---	MEMCS	Data15
30	RDY	I	---		---	MEMCS	Ready
31	EA0	O	---		1'b0	MEMCS	Address0
32	EA1	O	---		1'b0	MEMCS	Address1
33	EA2	O	---		1'b0	MEMCS	Address2
34	EA3	O	---		1'b0	MEMCS	Address3
35	EA4	O	---		1'b0	MEMCS	Address4
36	EA5	O	---		1'b0	MEMCS	Address5
37	EA6	O	---		1'b0	MEMCS	Address6
38	EA7	O	---		1'b0	MEMCS	Address7
39	EA8	O	---		1'b0	MEMCS	Address8
40	EA9	O	---		1'b0	MEMCS	Address9
41	EA10	O	---		1'b0	MEMCS	Address10
42	EA11	O	---		1'b0	MEMCS	Address11
43	EA12	O	---		1'b0	MEMCS	Address12
44	EA13	O	---		1'b0	MEMCS	Address13
45	EA14	O	---		1'b0	MEMCS	Address14
46	EA15	O	---		1'b0	MEMCS	Address15
47	EA16	O	---		1'b0	MEMCS	Address16
48	EA17	O	---		1'b0	MEMCS	Address17
49	EA18	O	---		1'b0	MEMCS	Address18
50	EA19	O	---		1'b0	MEMCS	Address19
51	EA20	O	---		1'b0	MEMCS	Address20
52	EA21	O	---		1'b0	MEMCS	Address21
53	EA22	O	---		1'b0	MEMCS	Address22
54	EA23	O	---		1'b0	MEMCS	Address23
55	EA24	O	---		1'b0	MEMCS	Address24

2.7. Drivability Adjustment Function

The LVCMOS I/O used in this SoC has the drivability adjustment function.

2.7.1. PD[65:0] Pins

It is possible to set “2mA, 4mA, 6mA, or 8mA” for each IO connected to the respective PD Pin. It is possible to set the IO drivability according to the drivability requested by the connected device.

2.7.2. Other Pins

It is possible to set the drivability for each IO group for the I/O other than the PD[65:0] pins. For example, it is possible to carry out drivability adjustment of RGMII I/F according to the IO voltage (VDDE) and the drivability requested by RGMII I/F PHY of the connection destination.

2.8. Pull Resistor Polarity Setting Function

This is a function for selecting the polarity of the pull resistor provided for each I/O.

2.8.1. PD[65:0] Pins

It is possible to set “Pull-OFF, Pull-UP, or Pull-DOWN” for each IO connected to its respective PD pin.

2.8.2. Other Pins

The polarities of the pull resistors connected to the I/O pins other than the PD [65:0] pins are fixed settings in the hardware mounting. Therefore, it is not possible to set the resistor polarity using this function.

2.9. External Pin Configuration Function

This is the function of reading in the polarities of the pull up/down resistors set in the board for the pins PD[63:56], and making it possible to allocate different functions according to the values read in by the software.

2.10. Pin Functions

2.10.1. Input Clock Pins

2.10.1.1. RTCLK

Table. 2-29: RTCLK

RTCLK

Input Frequency[MHz]	0.032768
Type (SE/Diff)	SE
Duty Cycle [%]	40-60
Period Jitter[ps]	-
C to C Jitter[ps]	-
RMS Jitter[ps]	-
ppm	±200 (when SSC=OFF)
SSC Input	○
SS(MIN) [%]	-3
SS(MAX) [%]	0
SS Freq(MAX) [kHz]	50
SS Waveform	Sine/Triangle
Interface	CMOS
Capacitance(MAX) [pF]	5

2.10.1.2. I2S_ECLK

Table. 2-30: I2S_ECLK

I2S_ECLK

Input Frequency[MHz]	24.576
Type (SE/Diff)	SE
Duty Cycle [%]	40-60
Period Jitter[ps]	-
C to C Jitter[ps]	-
RMS Jitter[ps]	-
ppm	±200
SSC Input	×
SS(MIN) [%]	-
SS(MAX) [%]	-
SS Freq(MAX) [kHz]	-
SS Waveform	-
Interface	CMOS
Capacitance(MAX) [pF]	5

2.10.1.3. SCLKDDR3

Table. 2-31: SCLKDDR3

SCLKDDR3

Input Frequency[MHz]	33.333
Type (SE/Diff)	SE
Duty Cycle [%]	40-60
Period Jitter[ps]	100ps(Pk-Pk)
C to C Jitter[ps]	-
RMS Jitter[ps]	-
ppm	±200(SSC=OFF)
SSC Input	○
SS(MIN) [%]	-3
SS(MAX) [%]	0
SS Freq(MAX) [kHz]	50
SS Waveform	Sine/Triangle
Interface	CMOS
Capacitance(MAX) [pF]	5

2.10.1.4. SCLK27M

Table. 2-32: SCLK27M

SCLK27M

Input Frequency[MHz]	27
Type (SE/Diff)	SE
Duty Cycle [%]	40-60
Period Jitter[ps]	100ps(Pk-Pk)
C to C Jitter[ps]	-
RMS Jitter[ps]	-
ppm	±200(SSC=OFF)
SSC Input	○
SS(MIN) [%]	-2
SS(MAX) [%]	0
SS Freq(MAX) [kHz]	50
SS Waveform	Sine/Triangle
Interface	CMOS
Capacitance(MAX) [pF]	5

2.10.1.5. USB3_REFCLK

Table. 2-33: USB3_REFCLK

USB3_REFCLK

Input Frequency[MHz]	20
Type (SE/Diff)	SE
Duty Cycle [%]	40-60
Period Jitter[ps]	-
C to C Jitter[ps]	-
RMS Jitter[ps]	4.3
ppm	±300
SSC Input	×
SS(MIN) [%]	-
SS(MAX) [%]	-
SS Freq(MAX) [kHz]	-
SS Waveform	-
Interface	CMOS
Capacitance(MAX) [pF]	5

2.10.1.6. ET_RXCLK

Table. 2-34: ET_RXCLK

ET_RXCLK

Input Frequency[MHz]	125±10%
Type (SE/Diff)	SE
Duty Cycle [%]	45-55
Period Jitter[ps]	-
C to C Jitter[ps]	-
RMS Jitter[ps]	-
ppm	±50
SSC Input	×
SS(MIN) [%]	-
SS(MAX) [%]	-
SS Freq(MAX) [kHz]	-
SS Waveform	-
Interface	CMOS
Capacitance(MAX) [pF]	5

2.10.1.7. SCLKMAIN

Table. 2-35: SCLKMAIN

SCLKMAIN

Input Frequency[MHz]	25
Type (SE/Diff)	SE
Duty Cycle [%]	40-60
Period Jitter[ps]	100ps(Pk-Pk)
C to C Jitter[ps]	-
RMS Jitter[ps]	-
ppm	±200
SSC Input	×
SS(MIN) [%]	-
SS(MAX) [%]	-
SS Freq(MAX) [kHz]	-
SS Waveform	-
Interface	CMOS
Capacitance(MAX) [pF]	5

2.10.1.8. SCLKCA15

Table. 2-36: SCLKCA15

SCLKCA15

Input Frequency[MHz]	25
Type (SE/Diff)	SE
Duty Cycle [%]	40-60
Period Jitter[ps]	100ps(Pk-Pk)
C to C Jitter[ps]	-
RMS Jitter[ps]	-
ppm	±200
SSC Input	×
SS(MIN) [%]	-
SS(MAX) [%]	-
SS Freq(MAX) [kHz]	-
SS Waveform	-
Interface	CMOS
Capacitance(MAX) [pF]	5

2.10.1.9. SCLKCA7

Table. 2-37: SCLKCA7

SCLKCA7

Input Frequency[MHz]	25
Type (SE/Diff)	SE
Duty Cycle [%]	40-60
Period Jitter[ps]	100ps(Pk-Pk)
C to C Jitter[ps]	-
RMS Jitter[ps]	-
ppm	±200
SSC Input	×
SS(MIN) [%]	-
SS(MAX) [%]	-
SS Freq(MAX) [kHz]	-
SS Waveform	-
Interface	CMOS
Capacitance(MAX) [pF]	5

2.10.1.10. PCIE0_REFCLKPI / PCIE0_REFCLKMI PCIE1_REFCLKPI / PCIE1_REFCLKMI

Table. 2-38: PCIE_REFCLK

PCIE0_REFCLKPI / PCIE1_REFCLKPI
PCIE0_REFCLKMI / PCIE1_REFCLKMI

Input Frequency[MHz]	100
Type (SE/Diff)	Diff
Duty Cycle [%]	40-60
Period Jitter[ps]	-
C to C Jitter[ps]	150
RMS Jitter[ps]	-
ppm	±300
SSC Input	○
SS(MIN) [%]	-0.5
SS(MAX) [%]	0
SS Freq(MAX) [kHz]	30～33
SS Waveform	-
Interface	HCSL/LVDS
Reference Clock Skew	Max 200
Capacitance(MAX) [pF]	5

3. Electrical characteristics

The electrical characteristics of MB86S72 are described in this Chapter.

3.1. Maximum Ratings

The maximum ratings are the limiting values that should not be exceeded even instantaneously. Application of a stress (voltage, current, temperature, etc.) exceeding the maximum ratings is likely to destroy the semiconductor device. Therefore, take care so that not even one parameter exceeds the ratings.

Table 3-1: Maximum ratings

Parameter	Symbol	Rating	Unit
Supply voltage	VDD, VDDA, VDD_CA7, VDD_CA15, VDD_SCB, VDD_FPD, VDD_DDR32, AVD_PLL[8:0], VPTX[3:0]_PCIE[1:0], VP_PCIE[1:0], VDU_USB30, VDU_USB31, VDN_USB30, VDN_USB31, AVDF2_USB30, AVDF2_USB31, AVDF2_USB2H, AVDF2_USB2HDC, AVDP_USB2H, AVDP_USB2HDC	-0.4 to 1.3	V
	VDE, VDEA, VDE15, VDE15A, VDE_FPD, VDE2, VPH_PCIE[1:0], AVD18_USB30, AVD18_USB31, AVD18_USB2H, AVD18_USB2HDC AVDH1, AVDH2	-0.5 to 2.5	
	VDE_SDIO[1:0] AVDF1_USB30, AVDF1_USB31, AVDF1_USB2H, AVDF1_USB2HDC	-0.5 to 4.6	
Input Voltage	V_I	-0.5 to VPTX_PCIE[1:0]/VP_PCIE[1:0]/ VDU_USB30/VDU_USB31 + 0.5 (≦1.3V) -0.5 to VDE15/VDE15A/AVD18_USB30/AVD18_USB31/ AVD18_USB2H/AVD18_USB2HDC + 0.5 (≦2.5V) -0.5 to 2.5V (VDE/VDEA/ VDE_FPD/VDE2) -0.5 to VDE_SDIO[1:0]/AVDF1_USB30/AVDF1_USB31/ AVDF1_USB2H/AVDF1_USB2HDC + 0.5V (≦4.6V)	V
Output Voltage	V_O	-0.5 to VPTX_PCIE[1:0]/VP_PCIE[1:0]/ VDU_USB30/VDU_USB31 + 0.5 (≦1.3V) -0.5 to VDE15/VDE15A/ AVD18_USB30/AVD18_USB31/ AVD18_USB2H/AVD18_USB2HDC + 0.5 (≦2.5V) -0.5 to 2.5V (VDE/VDEA/ VDE_FPD/VDE2) -0.5 to VDE_SDIO[1:0]/AVDF1_USB30/AVDF1_USB31/ AVDF1_USB2H/AVDF1_USB2HDC + 0.5V (≦4.6V)	V
Storage Temperature	T_{ST}	-55 to 125	℃
Junction Temperature	T_j	0 to 110	℃

3.2. Recommended Operating Conditions

The recommended operating conditions are the recommended values that guarantee normal logical operation of the device. That is, as long as the device is used within the range of the recommended operating conditions, the electrical characteristics (DC characteristics and AC characteristics) described later are guaranteed to be satisfied.

Table 3-2: Recommended operating conditions (1)

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
VDE, VDEA, VDE_FPD, VDE2,	Power Supply Voltage	1.700	1.800	1.950	V
VDE15, VDE15A	Power Supply Voltage	1.425	1.500	1.575	V
	Power Supply Voltage	1.283	1.350	1.450	V *1
VDE_SDIO[1:0]	Power Supply Voltage	1.700	1.800	1.950	V
	Power Supply Voltage	3.000	3.300	3.450	V *2
VDD, VDDA, VDD_SCB	Power Supply Voltage	0.855	0.900	0.945	V
VDD_CA7, VDD_CA15	Power Supply Voltage	0.855	0.900	0.945	V
	Power Supply Voltage	0.980	1.010	1.050	V *3
AVD_PLL[8:0]	Power Supply Voltage	0.855	0.900	0.945	V
	Ripple (peak-peak)			50	mV ppmax
VPTX_PCIE[1:0]	Power Supply Voltage	0.855	0.900	0.945	V
	Ripple (peak-peak)			30	mV ppmax
VPH_PCIE[1:0]	Power Supply Voltage	1.674	1.800	1.926	V
	Ripple (peak-peak)			30	mV ppmax
VDU_USB30, VDU_USB31	Power Supply Voltage	0.850	0.900	1.000	V
	Ripple (peak-peak)			30	mV ppmax
VDN_USB30, VDN_USB31	Power Supply Voltage	0.850	0.900	1.000	V
	Ripple (peak-peak)			50	mV ppmax
AVDF1_USB30, AVDF1_USB31	Power Supply Voltage	3.000	3.300	3.600	V
AVDF2_USB30, AVDF2_USB31	Power Supply Voltage	0.850	0.900	0.990	V
	Ripple (peak-peak)			50	mV ppmax
AVDP_USB30, AVDP_USB31	Power Supply Voltage	0.850	0.900	0.990	V
	Ripple (peak-peak)			50	mV ppmax
AVD18_USB30, AVD18_USB31	Power Supply Voltage	1.700	1.800	1.900	V
	Ripple (peak-peak)			50	mV ppmax
AVDF1_USB2H, AVDF1_USB2HDC	Power Supply Voltage	3.000	3.300	3.600	V
AVDF2_USB2H, AVDF2_USB2HDC	Power Supply Voltage	0.850	0.900	0.990	V
	Ripple (peak-peak)			50	mV ppmax
AVDP_USB2H, AVDP_USB2HDC	Power Supply Voltage	0.850	0.900	0.990	V
	Ripple (peak-peak)			50	mV ppmax
AVD18_USB2H, AVD18_USB2HDC	Power Supply Voltage	1.700	1.800	1.900	V
	Ripple (peak-peak)			50	mV ppmax

*1 DDR3L mode
*2 Do not use SDIO#0 and SDIO#1 simultaneously at 3.3V.
*3 Over Drive mode

Table 3-3: Recommended operating conditions (2)

Parameter		Symbol	Rating			Unit
			Min.	Typ.	Max.	
Input Voltage (High Level)	1.8V CMOS (Normal)	VIH	VDE/VDEA/ VDE_FPD/VDE2 x 0.650	-	VDE/VDEA/ VDE_FPD/VDE2 + 0.300	V
Input Voltage (Low Level)		VIL	-0.300	-	VDE/VDEA/ VDE_FPD/VDE2 x 0.350	V
Input Voltage (High Level)	1.8V CMOS (Schmitt)	VIH	VDE/VDEA/ VDE_FPD/VDE2 x 0.700	-	VDE/VDEA/ VDE_FPD/VDE2 + 0.300	V
Input Voltage (Low Level)		VIL	-0.300	-	VDE/VDEA/ VDE_FPD/VDE2 x 0.300	V
Input Voltage (High Level)	3.3V SDIO	VIH	VDE_SDIO[1:0] x 0.625	-	VDE_SDIO[1:0] + 0.300	V
Input Voltage (Low Level)		VIL	-0.300	-	VDE_SDIO[1:0] x 0.250	V
Input Voltage (High Level)	1.8V SDIO	VIH	1.270	-	2.000	V
Input Voltage (Low Level)		VIL	-0.300	-	0.580	V
Input Voltage (High Level)	eMMC	VIH	VDE x 0.65	-	VDE + 0.30	V
Input Voltage (Low Level)		VIL	-0.30	-	VDE x 0.35	V
Input Voltage (High Level)	I2C	VIH	VDE2 x 0.7	-	1.950	V
Input Voltage (Low Level)		VIL	-0.500	-	VDE2 x 0.3	V
Termination Voltage	DDR3/DDR3L	VTT	-	VDE15/2	-	V
Reference Voltage		$Vref_{(DC)}$	VDE15 x 0.475	-	VDE15 x 0.525	V
Input Voltage (High Level, Single, DC)	DDR3	$VIH_{(DC)}$	Vref(DC) + 0.1	-	VDE15	V
Input Voltage (Low Level, Single, DC)		$VIL_{(DC)}$	VSS – 0.3	-	Vref(DC) – 0.1	V
Input Voltage (High Level, Single, DC)	DDR3L	$VIH_{(DC)}$	Vref(DC) + 0.09	-	VDE15	V
Input Voltage (Low Level, Single, DC)		$VIL_{(DC)}$	VSS – 0.3	-	Vref(DC) – 0.09	V
Input Voltage (High Level, Single, AC)	DDR3	$VIH_{(AC)}$	Vref(DC) + 0.175	-	-	V
Input Voltage (Low Level, Single, AC)		$VIL_{(AC)}$	-	-	Vref(DC) – 0.175	V
Input Voltage (High Level, Single, AC)	DDR3L	$VIH_{(AC)}$	Vref(DC) + 0.160	-	-	V
Input Voltage (Low Level, Single, AC)		$VIL_{(AC)}$	-	-	Vref(DC) – 0.160	V
Operating ambient temperature		T_a	0	25	70	°C
Junction Temperature		T_j	0	25	110	°C

3.3. Power Consumption

MACRO name	Power supply PIN	Typ	Max	Unit	Notes
IO Cell	VDEA	0.4	1	mW	
	VDE	23.40	27.78	mW	
	VDE2	0.26	0.29	mW	
	VDE15A	62.18	77.63	mW	
	VDE15	1395.29	1732.44	mW	DDR3 1600Mbps
	VDE15	1010.5	1271.6	mW	DDR3L 1333Mbps
FPDLink	VDE_FPD	40.83	58.18	mW	
SDIO#0	VDE_SDIO0	18.32	22.09	mW	
SDIO#1	VDE_SDIO1	18.32	22.09	mW	
Logic core	VDDA	2.0	20	mW	
	VDD	1462.0	3839.0	mW	
	VDD_SCB	613.0	1740.0	mW	
Cortex-A7	VDD_CA7	225.0	655.0	mW	1200MHz
Cortex-A15	VDD_CA15	2516.0	4220.0	mW	1600MHz
FPDLink	VDD_FPD	2.0	47.0	mW	
PLL	AVD_PLL8	1.89	2.37	mW	
	AVD_PLL7	1.89	2.37	mW	
	AVD_PLL5	1.62	1.89	mW	
	AVD_PLL4	0.81	1.14	mW	
	AVD_PLL3	1.89	2.37	mW	
	AVD_PLL2	1.62	1.89	mW	
	AVD_PLL1	2.79	3.41	mW	
DDR PLL	VAA_PLL1	45.9	70.2	mW	
	VAA_PLL2	30.6	46.8	mW	
PCIE#0	VPTX_PCIE0	54.2	80.1	mW	
	VPH_PCIE0	68.0	107.1	mW	
	VP_PCIE0	85.5	123.8	mW	
PCIE#1	VPTX_PCIE1	54.2	80.1	mW	
	VPH_PCIE1	68.0	107.1	mW	
	VP_PCIE1	85.5	123.8	mW	
USB3.0#0	VDU_USB30	28.0	69.0	mW	
	VDN_USB30	19.0	55.0	mW	
	AVDF1_USB30	-	11.5	mW	
	AVDF2_USB30	-	0.82	mW	
	AVD18_USB30	-	50.7	mW	
	AVDP_USB30	-	6.2	mW	
USB3.0#1	VDU_USB31	28.0	69.0	mW	
	VDN_USB31	19.0	55.0	mW	
	AVDF1_USB31	-	11.5	mW	
	AVDF2_USB31	-	0.82	mW	
	AVD18_USB31	-	50.7	mW	
	AVDP_USB31	-	6.2	mW	
USB2.0#Host	AVDF1_USB2H	-	11.5	mW	
	AVDF2_USB2H	-	0.82	mW	
	AVD18_USB2H	-	50.7	mW	
	AVDP_USB2H	-	6.2	mW	

MACRO name	Power supply PIN	Typ	Max	Unit	Notes
USB2.0#Host/Device	AVDF1_USB2HDC	-	11.5	mW	
	AVDF2_USB2HDC	-	0.82	mW	
	AVD18_USB2HDC	-	50.7	mW	
	AVDP_USB2HDC	-	6.2	mW	
Temperature Sensor	AVDH_CA15_0	0.18	0.22	mW	
	AVDH_CA15_1	0.18	0.22	mW	
	AVDH_CA7_0	0.18	0.22	mW	
	AVDH_CA7_1	0.18	0.22	mW	
	AVDH_DDR	0.18	0.22	mW	
	AVDH_MALI	0.18	0.22	mW	

3.4. DC Characteristics

The DC characteristics of each I/O buffer are described in this Section.

3.4.1. Fail-Safe Multi-Drive I/O Buffer

Table. 3-4: Fail-Safe Multi-Drive I/O Buffer

Parameter	Symbol	Condition		Rating			Unit
				Min.	Typ.	Max.	
H level output voltage	VOH	2mA buffer	IOH = -2mA	VDE/VDEA/VDE2 - 0.4	—	VDE/VDEA/ VDE2	V
		4mA buffer	IOH = -4mA				
		6mA buffer	IOH = -6mA				
		8mA buffer	IOH = -8mA				
L level output voltage	VOL	2mA buffer	IOL = 2mA	0	—	0.4	V
		4mA buffer	IOL = 4mA				
		6mA buffer	IOL = 6mA				
		8mA buffer	IOL = 8mA				
Pull-Up resistance	Rpu	@VIL=0V		55	75	111	kΩ
Pull-Down resistance	Rpd	@VIH = VDE/VDEA/VDE2		53	75	132	kΩ
Input leak	IL	—		-10	—	+10	uA

3.4.1.1. Fail-Safe Multi-Drive I/O Buffer V - I Characteristics (2mA buffer)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE/VDEA/VDE2 = 1.65 V
	TYP: Process = Typical	T_J = 25°C	VDE/VDEA/VDE2 = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE/VDEA/VDE2 = 1.95 V

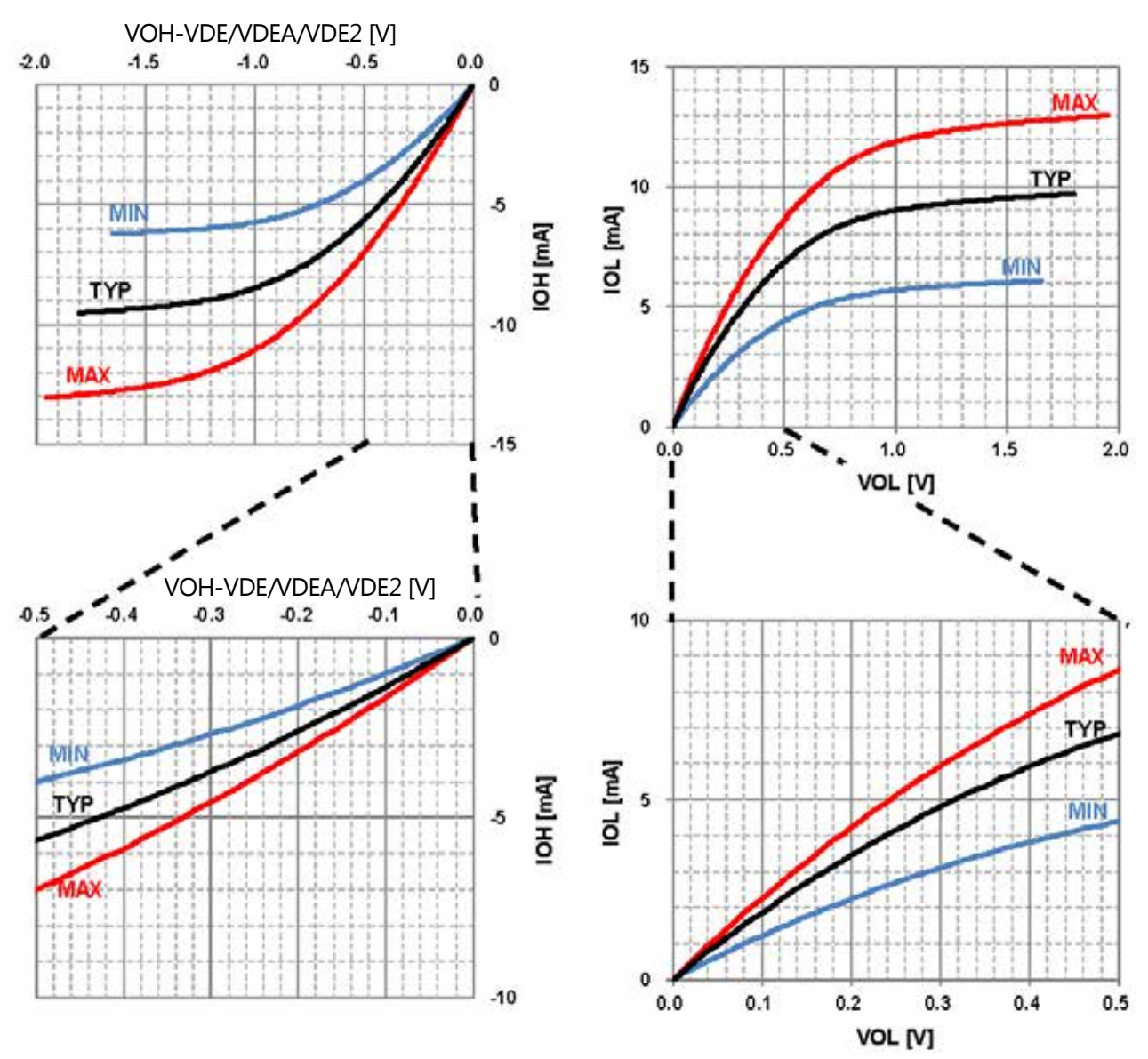


Figure 3-1: Fail-Safe Multi-Drive I/O Buffer V - I Characteristics (2mA buffer)

3.4.1.2. Fail-Safe Multi-Drive I/O Buffer V - I Characteristics (4mA buffer)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE/VDEA/VDE2 = 1.65 V
	TYP: Process = Typical	T_J = 25°C	VDE/VDEA/VDE2 = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE/VDEA/VDE2 = 1.95 V

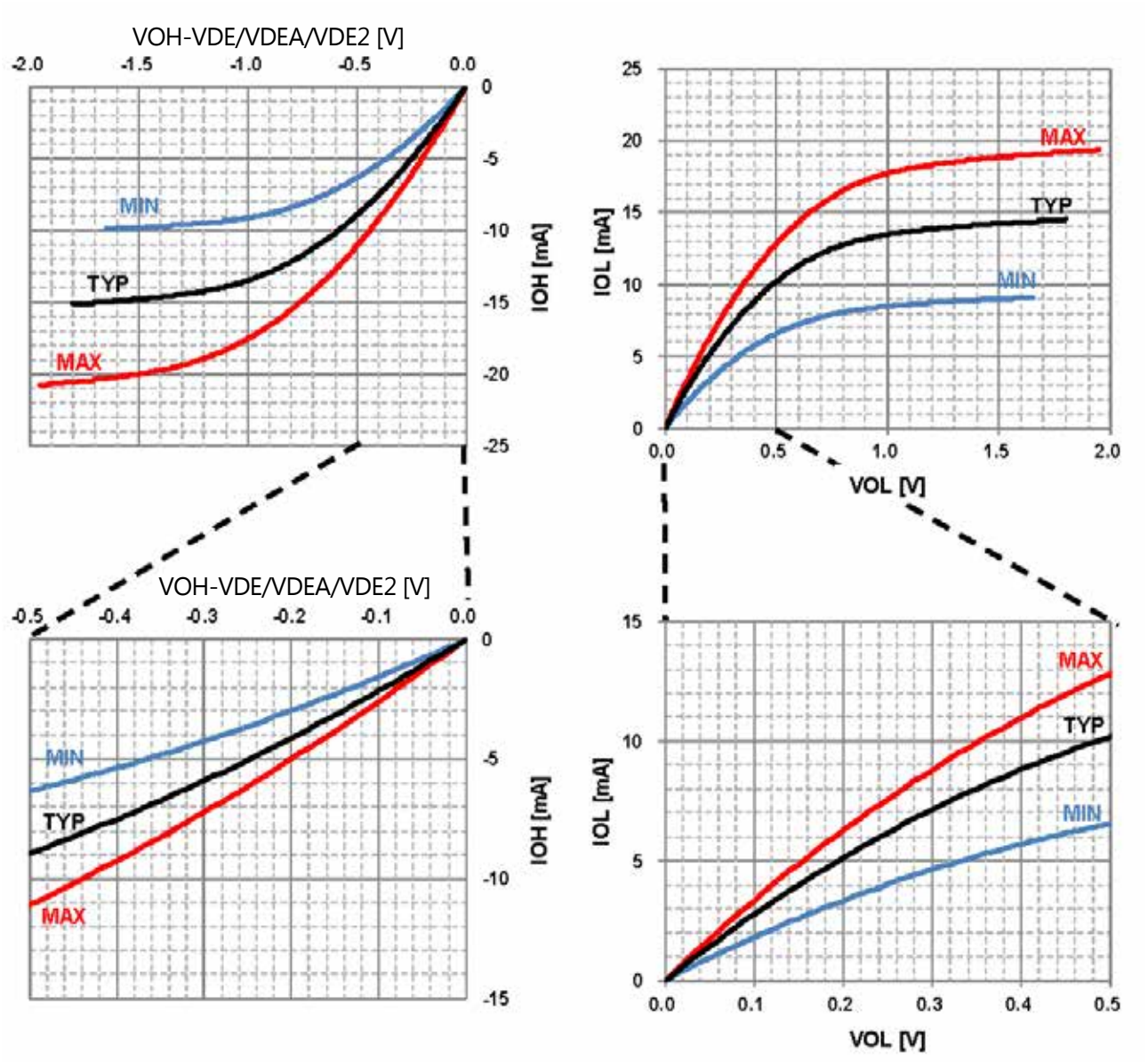


Figure 3-2: Fail-Safe Multi-Drive I/O Buffer V - I Characteristics (4mA buffer)

3.4.1.3. Fail-Safe Multi-Drive I/O Buffer V - I Characteristics (6mA buffer)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE/VDEA/VDE2 = 1.65 V
	TYP: Process = Typical	T_J = 25°C	VDE/VDEA/VDE2 = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE/VDEA/VDE2 = 1.95 V

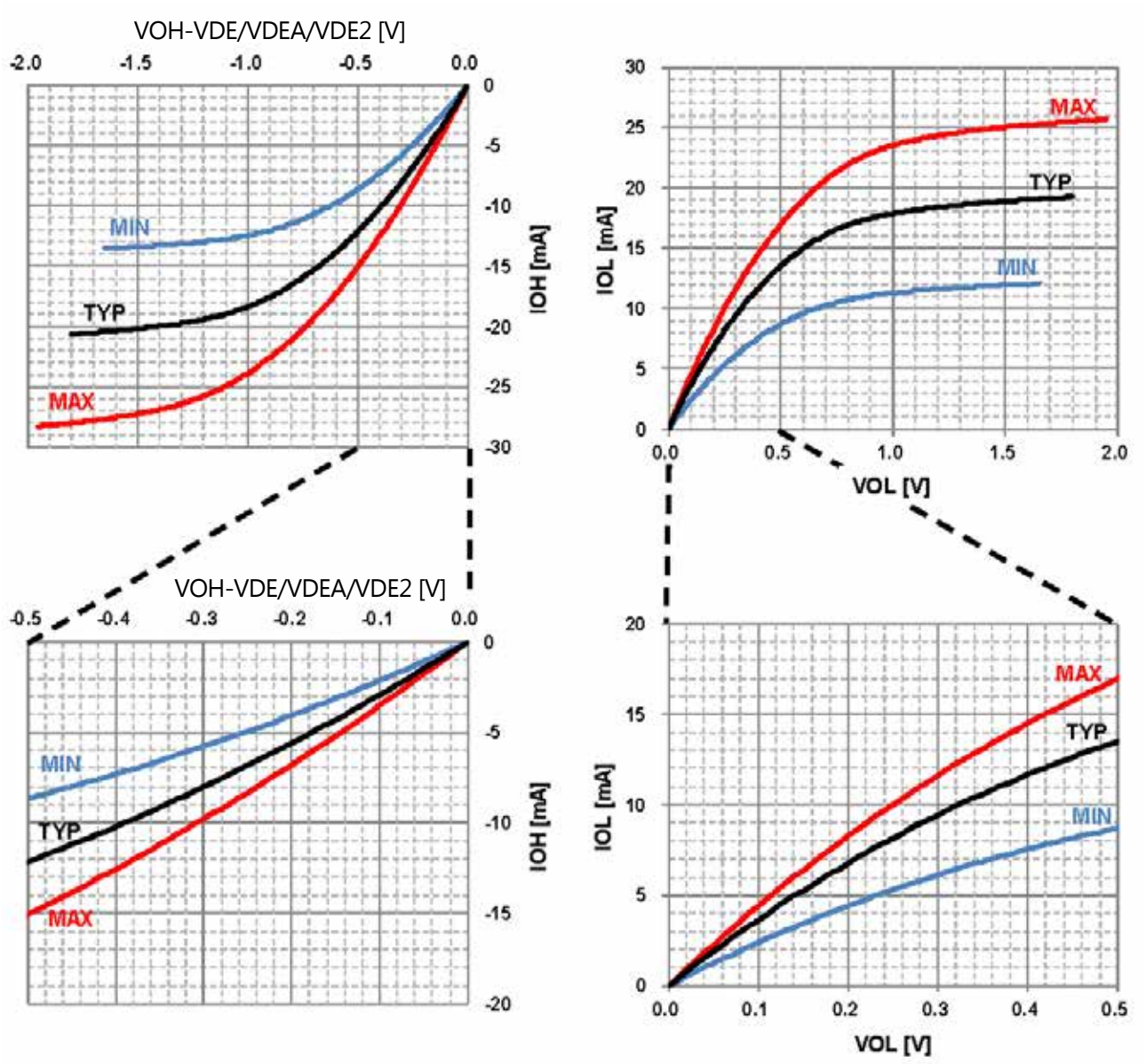


Figure 3-3: Fail-Safe Multi-Drive I/O Buffer V - I Characteristics (6mA buffer)

3.4.1.4. Fail-Safe Multi-Drive I/O Buffer V - I Characteristics (8mA buffer)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE/VDEA/VDE2 = 1.65 V
	TYP: Process = Typical	T_J = 25°C	VDE/VDEA/VDE2 = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE/VDEA/VDE2 = 1.95 V

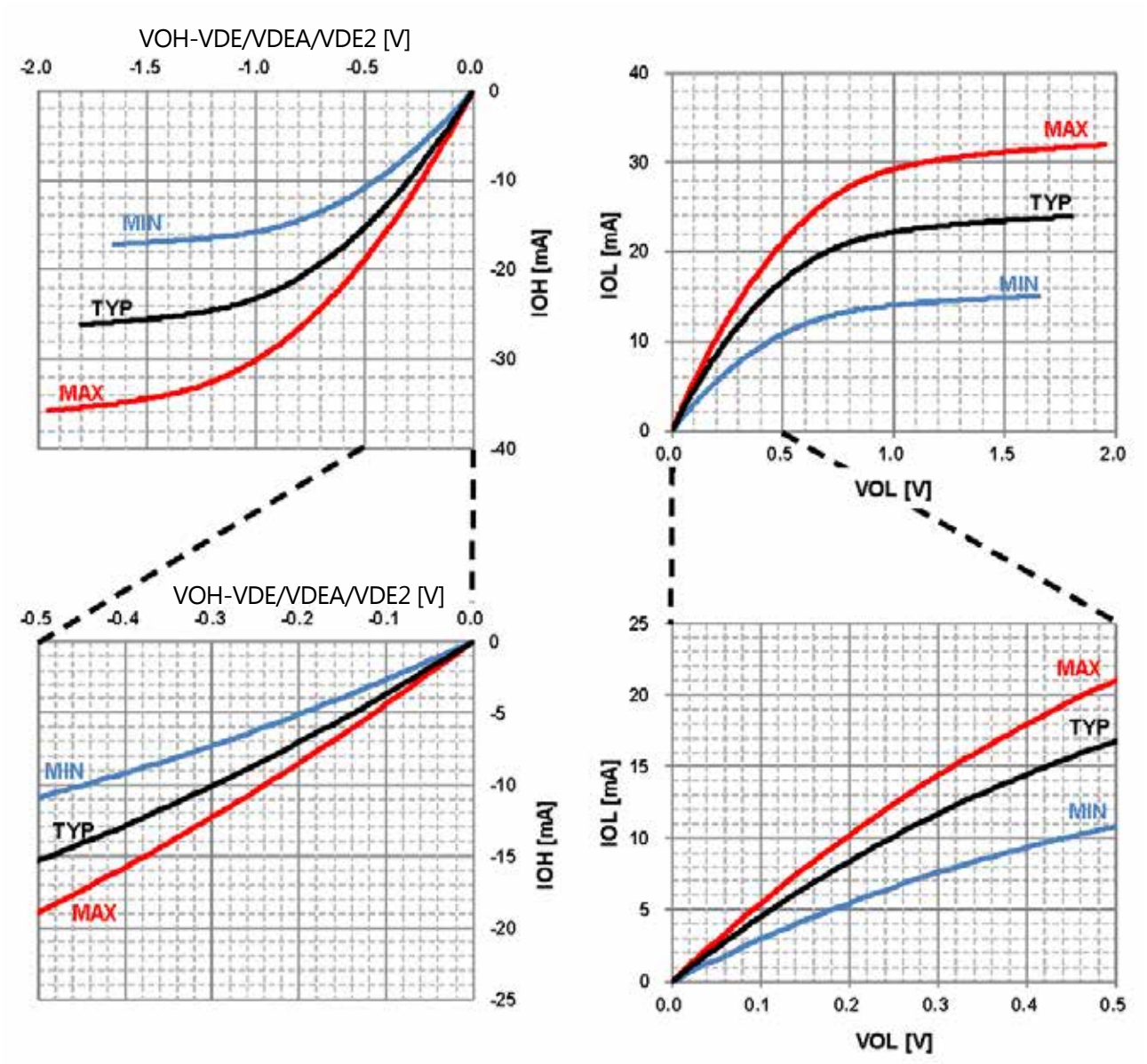


Figure 3-4: Fail-Safe Multi-Drive I/O Buffer V - I Characteristics (8mA buffer)

3.4.2. I²C Fast Mode I/O Buffer

Table. 3-5: I²C Fast Mode I/O Buffer

Parameter	Symbol	Fast Mode		Standard Mode		Unit
		Min.	Max.	Min.	Max.	
L level output voltage Sink current 3[mA] VDE2<2[V]	VOL	0	0.2 * VDE2	Not specified	Not specified	V
Output slew rate VIH(min.) to VIL(max.) Bus capacitance 10 to 400[pF]	tof	20 + 0.1 * Cb (*1)	250	—	250	ns
Leak current Input voltage 0.1 to 0.9*VDE2(max.)	Ii	-10	10	-10	10	uA
I/O pin capacitance	Ci	—	10	—	10	pF

(*1) Cb: Capacitance of one bus line (unit: pF)

Not compliant with NXP Corp. I²C-bus specification and user manual Rev4.

3.4.2.1. V - I CHARACTERISTICS

Conditions	MIN: Process = Slow	T_J = 110°C	VDE2 = 1.65 V
	TYP: Process = Typical	T_J = 25°C	VDE2 = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE2 = 1.95 V

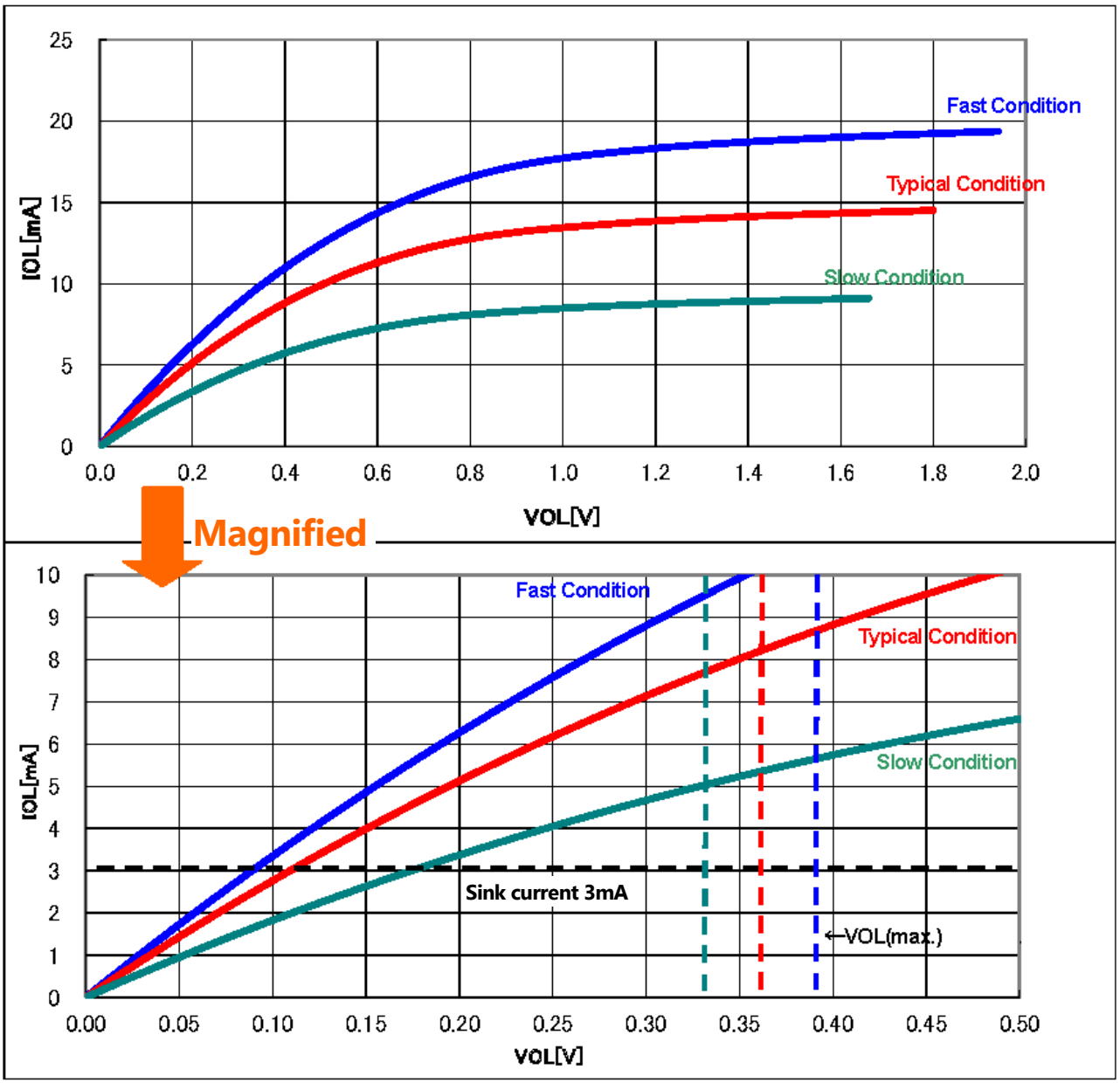


Figure 3-5: V - I Characteristics

3.4.3. I^2C High Speed Mode (Fail-Safe Multi-Drive I/O Buffer)

Table. 3-6: I^2C High Speed Mode (Fail-Safe Multi-Drive I/O Buffer)

Parameter	Symbol	Condition		Rating			Unit
				Min.	Typ.	Max.	
H level output voltage	VOH	4mA buffer	IOH = -4mA	VDE - 0.4	—	VDE	V
L level output voltage	VOL	4mA buffer	IOL = 4mA	0	—	0.4	V
Bus capacitance	Cb			—	—	100	pF
Input leak	IL	—		-10	—	+10	uA

3.4.3.1. V - I CHARACTERISTICS

Conditions	MIN: Process = Slow	T_J = 110°C	VDE = 1.65 V
	TYP: Process = Typical	T_J = 25°C	VDE = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE = 1.95 V

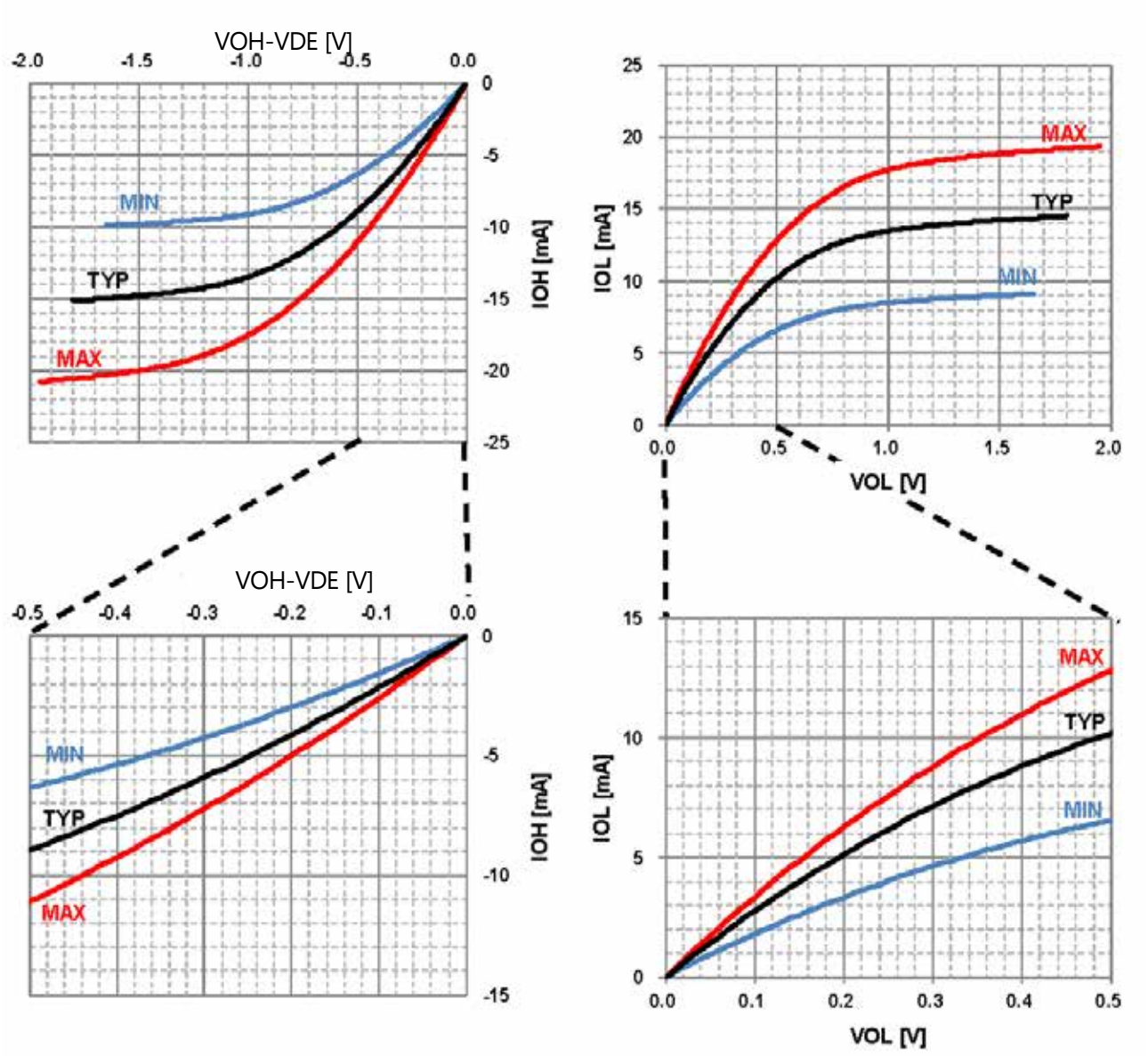


Figure 3-6: V - I Characteristics

3.4.4. LVDS Driver Cell

Table. 3-7: LVDS Driver Cell

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Output offset voltage	Vos	Rload = 100Ω	1.075	1.2	1.325	V
Output differential voltage	|Vod|	Rload = 100Ω	230	340	490	mV

3.4.4.1. Output signal levels

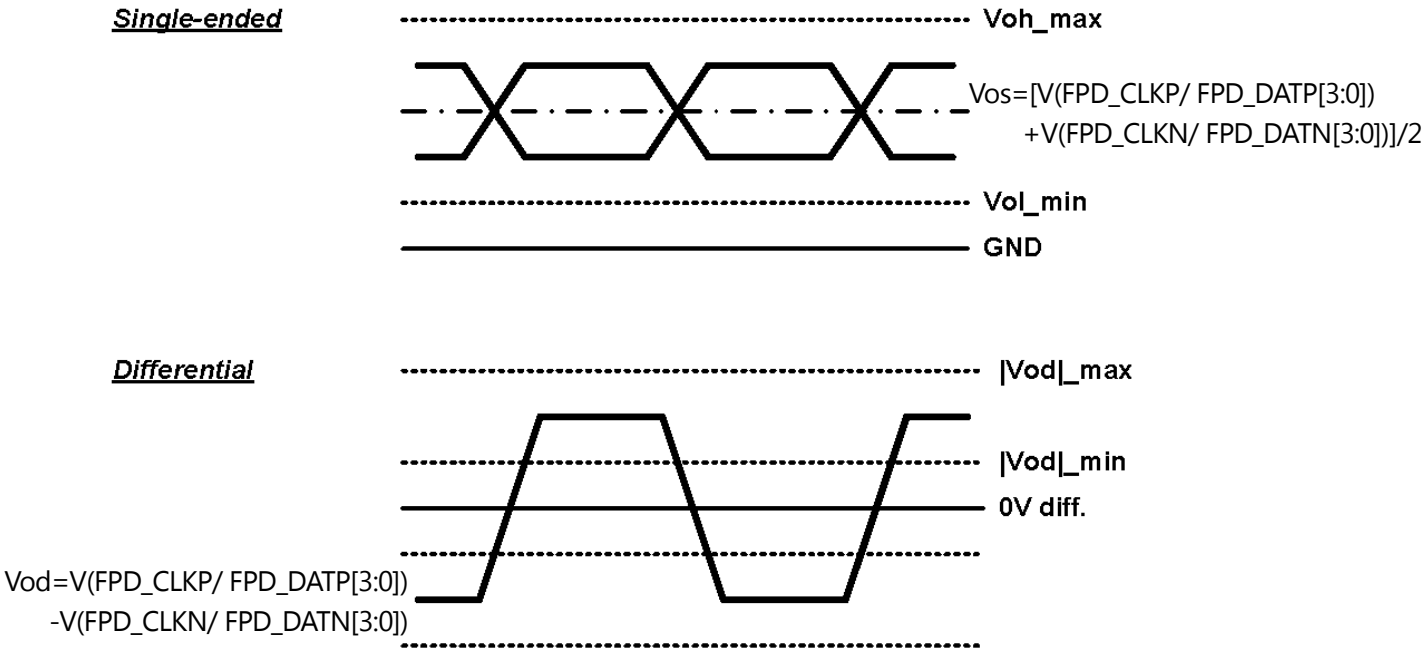


Figure. 3-7: Output signal levels

3.4.4.2. Measurement circuit of output signal levels

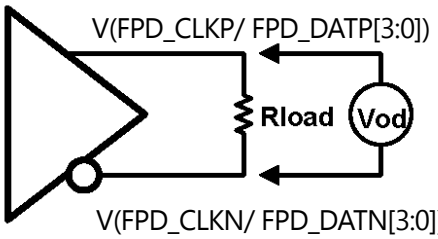


Figure. 3-8: Measurement circuit of output signal levels

3.4.5. DDR3 Mode

3.4.5.1. DC Specifications

The following table provides input and output DC threshold values and On-Die-Termination (ODT) recommended values. The conditions for the output threshold values are unterminated outputs loaded with 1 pF capacitor load. The ODT values are measured after impedance calibration.

Table. 3-8 :DDR3 Mode – DC Specifications

Symbol	Parameter	Min	Nom	Max	Units
VIH_DC	DC input voltage High	VREF + 0.1		VDDQ	V
VIL_DC	DC input voltage Low	VSSQ – 0.3		VREF – 0.1	V
VOH	DC output logic High	0.8 * VDDQ			V
VOL	DC output logic Low			0.2 * VDDQ	V
RTT	Input termination resistance(ODT) to VDDQ/2	100	120	140	ohm
		54	60	66	
		36	40	44	

3.4.5.2. Current Specifications

The following table provides the current value ranges of the power supply and the output ignoring the current direction (absolute value), output impedance calibrated to Zout=34 ohms. The values are simulated parameters; in the event of test silicon, this parameter may not be measured. The leakage current is specified at 125C junction temperature.

Table. 3-9:DDR3 Mode – Current Specifications

Symbol	Parameter	Min	Nom	Max	Units
IOHL_34_120	PAD pin, 34 ohm Output source/sink DC current, Rtt=120	4.73	5.01	5.30	mA
IOHL_34_60	PAD pin, 34 ohm Output source/sink DC current, Rtt=60	7.82	8.33	8.85	mA
IOHL_34_40	PAD pin, 34 ohm Output source/sink DC current, Rtt=40	9.99	10.66	11.35	mA
IOHL_50_120	PAD pin, 50 ohm Output source/sink DC current, Rtt=120	4.21	4.48	4.74	mA
IOHL_50_60	PAD pin, 50 ohm Output source/sink DC current, Rtt=60	6.48	6.92	7.34	mA
IOHL_50_40	PAD pin, 50 ohm Output source/sink DC current, Rtt=40	7.88	8.44	8.95	mA
IDDQ_OFF	VDDQ standby current; ODT OFF	0.23	0.5	189	uA
IVAA_PLL_OFF	VAA_PLL standby current; ODT OFF	0.00	0.00	1.28	uA
IDDQ_DRV0_34_60	Output Low Drv/Rtt=34/60, IDDQ DC current	0.00	0.00	0.21	mA
IDDQ_DRV1_34_60	Output High Drv/Rtt=34/60, IDDQ DC current	7.83	8.23	8.78	mA
IDDQ_RCV0_34_60	Input Low ODT/Drv=60/34, IDDQ DC current	10.56	11.32	11.88	mA
IDDQ_RCV1_34_60	Input High ODT/Drv=60/34, IDDQ DC current	2.48	2.67	2.94	mA
ILEAK	Input leakage current, SSTL mode, unterminated	0.01	0.03	1.92	uA

3.4.5.3. DC Receive Mode Power Specifications

The following table provides the DC power only for the I/O in receive mode for different system configurations. The parameters are simulated values; in the event of test silicon, this parameter may not be measured. For the total power, the designer should sum DC power and AC power.

Table. 3-10:DC Receive Mode Power Dissipation – DDR3 Mode

Symbol	Parameter	Min	Nom	Max	Units
PRCV	Input mode DC power dissipation, ODT=OFF	0.00	0.00	0.29	mW
PRCV	Input mode DC power dissipation, ODT/Drv=120/34	6.01	7.44	9.56	mW
PRCV	Input mode DC power dissipation, ODT/Drv=60/34	11.61	13.91	16.20	mW
PRCV	Input mode DC power dissipation, ODT/Drv=40/34	16.90	19.88	22.89	mW
PRCV	Input mode DC power dissipation, ODT/Drv=120/50	5.81	7.09	9.03	mW
PRCV	Input mode DC power dissipation, ODT/Drv=60/50	11.17	13.17	15.24	mW
PRCV	Input mode DC power dissipation, ODT/Drv=40/50	16.28	18.89	21.60	mW
PRCV	Input mode DC power dissipation, VDD rail	0.14	0.29	43.41	uW
PRCV	Input mode DC power dissipation, VAA_PLL rail	0.30	0.69	1.48	mW

3.4.5.4. DC Drive Mode Power Specifications

The following table provides the DC power only for the I/O in drive mode for different system configurations. The parameters are simulated values; in the event of test silicon, this parameter may not be measured. For the total power, the designer should sum DC power and AC power. The standby mode power is specified for 125 degC junction temperature.

Table. 3-11:DC Drive Mode Power Dissipation (PDR=0) – DDR3 Mode

Symbol	Parameter	Min	Nom	Max	Units
PDRV	Output mode DC power dissipation, Rtt=OFF	0.00	0.00	0.33	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=34/120	0.66	0.75	1.17	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=34/60	1.86	2.09	2.66	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=34/40	3.10	3.45	4.15	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=50/120	0.85	0.96	1.37	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=50/60	2.09	2.32	2.88	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=50/40	3.13	3.48	4.18	mW
PDRV	Output mode DC power dissipation, VDD rail	0.10	0.29	43.95	uW
PDRV	Output mode DC power dissipation, VAA_PLL rail	0.29	0.69	1.50	mW

Table. 3-12:DC Drive Mode Power Dissipation (PDR=1) – DDR3 Mode

Symbol	Parameter	Min	Nom	Max	Units
PDRV	Output mode DC power dissipation, Rtt=OFF	0.00	0.00	0.33	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=34/120	0.66	0.75	1.17	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=34/60	1.86	2.09	2.66	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=34/40	3.10	3.45	4.15	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=50/120	0.85	0.96	1.37	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=50/60	2.09	2.32	2.88	mW
PDRV	Output mode DC power dissipation, Drv/Rtt=50/40	3.13	3.48	4.18	mW
PDRV	Output mode DC power dissipation, VDD rail	0.09	0.28	43.45	uW
PSTB	Standby mode DC power dissipation (VDDQ rail)	0.33	0.75	297.68	uW
PDRV	Output mode DC power dissipation, VAA_PLL rail	0	0.00	2.53	uW

Table. 3-13:IO Cells Power Specifications – DDR3 Mode (ZQ_OFF, PD are asserted for PZQ)

Symbol	Parameter	Min	Nom	Max	Units
PWRQ_PZQ_STBY	PZQ VDDQ Standby Power	0	0.01	10.36	uW
PWR_PZQ_STBY	PZQ VDD Standby Power	0	0.03	3.61	uW
PWRQ_PRETPOCX_STBY	PRETPOCX VDDQ Standby Power	0	0.01	7.67	uW
PWR_PRETPOCX_STBY	PRETPOCX VDD Standby Power	0	0	0	uW
PWRQ_PRETPOCC_STBY	PRETPOCC VDDQ Standby Power	0	0.01	7.37	uW
PWR_PRETPOCC_STBY	PRETPOCC VDD Standby Power	0	0	0	uW
PWRQ_PVREF_STBY	PVREF VDDQ Standby Power	0	0.03	30.49	uW
PWR_PVREF_STBY	PVREF VDD Standby Power	0	50.69	228.70	uW
PWRQ_PVDDQ_ESD_STBY	PVDDQ ESD VDDQ Standby Power	0	0.00	0.0021	uW
PWR_PVDDQ_ESD_STBY	PVDDQ ESD VDD Standby Power	0	0	0	uW
PWRQ_PVDDQ_CAP_STBY	PVDDQ CAP VDDQ Standby Power	0	0.05	48.5	uW
PWR_PVDDQ_CAP_STBY	PVDDQ CAP VDD Standby Power	0	0	0	uW
PWRQ_PVDD_ESD_STBY	PVDD ESD VDDQ Standby Power	0	0	0.0016	uW
PWR_PVDD_ESD_STBY	PVDD ESD VDD Standby Power	1	2.53	11.3	uW
PWRQ_PVDD_CAP_STBY	PVDD CAP VDDQ Standby Power	0	0	0.0016	uW
PWR_PVDD_CAP_STBY	PVDD CAP VDD Standby Power	0	0	0	uW
PWRQ_PVAA_PLL_STBY	PVAA_PLL VAA_PLL Standby Power	2.62	3.24	3.92	uW
PWR_PVAA_PLL_STBY	PVAA_PLL VDDQ Standby Power	2.03	2.25	2.48	uW
PWR_PVAA_PLL_STBY	PVAA_PLL ESD VDD Standby Power	0.66	0.81	0.98	uW
PWR_PVSS_STBY	PVSS VDDQ Standby Power	0	0.045	49.3	uW
PWR_PVSS_STBY	PVSS ESD VDD Standby Power	0	0	0	uW
PWR_PVSSQ_STBY	PVSSQ VDDQ Standby Power	0	0	0	uW
PWR_PVSSQ_STBY	PVSSQ ESD VDD Standby Power	0	0	0	uW

Table. 3-14:PZQ Power Specifications – DDR3 Mode (ZQ_OFF deasserted)

Symbol	Parameter	Min	Nom	Max	Units
PDR_VQ_34	VDDQ Power ZQ_OFF deasserted – drive 34	34.38	39.45	44.91	mW
PDR_VQ_40	VDDQ Power ZQ_OFF deasserted – drive 40	30.11	34.34	39.45	mW
PDR_VQ_50	VDDQ Power ZQ_OFF deasserted – drive 50	23.89	27.30	31.47	mW
PRC_VQ_40	VDDQ Power ZQ_OFF deasserted – odt 40	19.24	22.55	25.89	mW
PRC_VQ_60	VDDQ Power ZQ_OFF deasserted – odt 60	14.36	17.02	19.98	mW
PRC_VQ_120	VDDQ Power ZQ_OFF deasserted – odt 120	9.61	11.41	14.18	mW
PRCV	VDD Power ZQ_OFF deasserted	0.01	8.30	17.83	uW

3.4.6. DDR3L Mode

3.4.6.1. DC Specifications

The following table provides input and output DC threshold values and On-Die-Termination (ODT) recommended values. The conditions for the output threshold values are un-terminated outputs loaded with 1 pF capacitor load. The ODT values are measured after impedance calibration.

Table. 3-15:DDR3L Mode – DC Specifications

Symbol	Parameter	Min	Nom	Max	Units
VIH(DC)	DC input voltage High	VREF + 0.09		VDDQ	V
VIL(DC)	DC input voltage Low	VSSQ – 0.3		VREF – 0.09	V
VOH	DC output logic High	0.8 * VDDQ			V
VOL	DC output logic Low			0.2 * VDDQ	V
RTT	Input termination resistance(ODT) to VDDQ/2	100	120	140	ohm
		54	60	66	
		36	40	44	

3.4.6.2. Current Specifications

The following table provides the current value ranges of the power supply and the output ignoring the current direction (absolute value), output impedance calibrated to Zout=34 ohms. The values are simulated parameters; in the event of test silicon, this parameter may not be measured. The leakage current is specified at 125C junction temperature.

Table. 3-16: Current Specifications – DDR3L Mode

Symbol	Parameter	Min	Nom	Max	Units
IOHL_34_120	PAD pin, 34 ohm Output source/sink DC current, Rtt=120	4.28	4.52	4.90	mA
IOHL_34_60	PAD pin, 34 ohm Output source/sink DC current, Rtt=60	7.09	7.51	8.19	mA
IOHL_34_40	PAD pin, 34 ohm Output source/sink DC current, Rtt=40	9.06	9.61	10.50	mA
IOHL_50_120	PAD pin, 50 ohm Output source/sink DC current, Rtt=120	3.84	4.07	4.39	mA
IOHL_50_60	PAD pin, 50 ohm Output source/sink DC current, Rtt=60	5.95	6.32	6.82	mA
IOHL_50_40	PAD pin, 50 ohm Output source/sink DC current, Rtt=40	7.25	7.71	8.31	mA
IDDQ_OFF	VDDQ standby current; ODT OFF	0.17	0.39	160.10	uA
IVAA_PLL_OFF	VAA_PLL standby current; ODT OFF	0	0.00	1.26	uA
IDDQ_DRV0_34_60	Output Low Drv/Rtt=34/60, IDDQ DC current	0.00	0.00	0.17	mA
IDDQ_DRV1_34_60	Output High Drv/Rtt=34/60, IDDQ DC current	7.09	7.42	8.13	mA
IDDQ_RCV0_34_60	Input Low ODT/Drv=60/34, IDDQ DC current	9.03	9.95	10.50	mA
IDDQ_RCV1_34_60	Input High ODT/Drv=60/34, IDDQ DC current	2.10	2.32	2.51	mA
ILEAK	Input leakage current, SSTL mode, unterminated	0	0.03	1.80	uA

3.4.6.3. DC Receive Mode Power Specifications

The following table provides the DC power only for the I/O in receive mode for different system configurations. The parameters are simulated values; in the event of test silicon, this parameter may not be measured. For the total power, the designer should sum DC power and AC power.

Table. 3-17:DC Receive Mode Power Dissipation – DDR3L Mode

Symbol	Parameter	Min	Nom	Max	Units
PRCV_OFF	Input mode DC power dissipation, ODT=OFF	0.00	0.00	0.23	mW
PRCV_34_120	Input mode DC power dissipation, ODT/Drv=120/34	4.90	6.07	7.75	mW
PRCV_34_60	Input mode DC power dissipation, ODT/Drv=60/34	8.98	10.96	13.20	mW
PRCV_34_40	Input mode DC power dissipation, ODT/Drv=40/34	13.12	15.71	19.31	mW
PRCV_50_120	Input mode DC power dissipation, ODT/Drv=120/50	4.75	5.81	7.34	mW
PRCV_50_60	Input mode DC power dissipation, ODT/Drv=60/50	8.67	10.43	12.44	mW
PRCV_50_40	Input mode DC power dissipation, ODT/Drv=40/50	12.71	15.02	18.24	mW
PRCV	Input mode DC power dissipation, VDD rail	0.13	0.29	43.47	uW
PRCV_VAA_PLL	Input mode DC power dissipation, VAA_PLL rail	0.28	0.69	1.53	mW

3.4.6.4. DC Drive Mode Power Specifications

The following table provides the DC power only for the I/O in drive mode for different system configurations. The parameters are simulated values; in the event of test silicon, this parameter may not be measured. For the total power, the designer should sum DC power and AC power. The standby mode power is specified for 125 degC junction temperature.

Table. 3-18:DC Drive Mode Power Dissipation (PDR=0) – DDR3L Mode

Symbol	Parameter	Min	Nom	Max	Units
PDRV_OFF	Output mode DC power dissipation, Rtt=OFF	0.00	0.00	0.25	mW
PDRV_34_120	Output mode DC power dissipation, Drv/Rtt=34/120	0.52	0.61	0.96	mW
PDRV_34_60	Output mode DC power dissipation, Drv/Rtt=34/60	1.49	1.69	2.22	mW
PDRV_34_40	Output mode DC power dissipation, Drv/Rtt=34/40	2.50	2.80	3.49	mW
PDRV_50_120	Output mode DC power dissipation, Drv/Rtt=50/120	0.68	0.76	1.13	mW
PDRV_50_60	Output mode DC power dissipation, Drv/Rtt=50/60	1.69	1.88	2.42	mW
PDRV_50_40	Output mode DC power dissipation, Drv/Rtt=50/40	2.55	2.83	3.53	mW
PDRV	Output mode DC power dissipation, VDD rail	0.10	0.29	44.03	uW
PDRV_VAA_PLL	Output mode DC power dissipation, VAA_PLL rail	0.27	0.69	1.54	mW

Table. 3-19:DC Drive Mode Power Dissipation (PDR=1) – DDR3L Mode

Symbol	Parameter	Min	Nom	Max	Units
PDRV_OFF	Output mode DC power dissipation, Rtt=OFF	0.00	0.00	0.25	mW
PDRV_34_120	Output mode DC power dissipation, Drv/Rtt=34/120	0.52	0.61	0.96	mW
PDRV_34_60	Output mode DC power dissipation, Drv/Rtt=34/60	1.49	1.69	2.22	mW
PDRV_34_40	Output mode DC power dissipation, Drv/Rtt=34/40	2.50	2.80	3.49	mW
PDRV_50_120	Output mode DC power dissipation, Drv/Rtt=50/120	0.68	0.76	1.13	mW
PDRV_50_60	Output mode DC power dissipation, Drv/Rtt=50/60	1.69	1.88	2.42	mW
PDRV_50_40	Output mode DC power dissipation, Drv/Rtt=50/40	2.55	2.83	3.53	mW
PDRV	Output mode DC power dissipation, VDD rail	0.09	0.28	43.52	uW
PSTBY_VDDQ	Standby mode DC power dissipation (VDDQ rail)	0	0.53	232.15	uW
PSTBY_VAA_PLL	Standby mode DC power dissipation (VAA_PLL rail)	0	0.00	2.49	uW

Table. 3-20: IO Cells Power Specifications – DDR3L Mode (ZQ_OFF, PD are asserted for PZQ)

Symbol	Parameter	Min	Nom	Max	Units
PWRQ_PZQ_STBY	PZQ VDDQ Standby Power	0	0.01	8.79	uW
PWR_PZQ_STBY	PZQ VDD Standby Power	0	0.03	3.61	uW
PWRQ_PRETPOCX_STBY	PRETPOCX VDDQ Standby Power	0	0.01	6.46	uW
PWR_PRETPOCX_STBY	PRETPOCX VDD Standby Power	0	0	0	uW
PWRQ_PRETPOCC_STBY	PRETPOCC VDDQ Standby Power	0	0.01	6.21	uW
PWR_PRETPOCC_STBY	PRETPOCC VDD Standby Power	0	0	0	uW
PWRQ_PVREF_STBY	PVREF VDDQ Standby Power	0	0.03	13.05	uW
PWR_PVREF_STBY	PVREF VDD Standby Power	0	50.69	228.70	uW
PWRQ_PVDDQ_ESD_STBY	PVDDQ ESD VDDQ Standby Power	0	0.0001	0.0014	uW
PWR_PVDDQ_ESD_STBY	PVDDQ ESD VDD Standby Power	0	0	0	uW
PWRQ_PVDDQ_CAP_STBY	PVDDQ CAP VDDQ Standby Power	0	0.036	41.8	uW
PWR_PVDDQ_CAP_STBY	PVDDQ CAP VDD Standby Power	0	0	0	uW
PWRQ_PVDD_ESD_STBY	PVDD ESD VDDQ Standby Power	0	0	0.0014	uW
PWR_PVDD_ESD_STBY	PVDD ESD VDD Standby Power	1	2.53	11.3	uW
PWRQ_PVDD_CAP_STBY	PVDD CAP VDDQ Standby Power	0	0	0.0014	uW
PWR_PVDD_CAP_STBY	PVDD CAP VDD Standby Power	0	0	0	uW
PWRQ_PVAA_PLL_STBY	PVAA_PLL VAA_PLL Standby Power	2.62	3.24	3.92	uW
PWR_PVAA_PLL_STBY	PVAA_PLL VDDQ Standby Power	1.65	1.82	2.1	uW
PWR_PVAA_PLL_STBY	PVAA_PLL ESD VDD Standby Power	0.66	0.81	0.98	uW
PWR_PVSS_STBY	PVSS VDDQ Standby Power	0	0.037	42.6	uW
PWR_PVSS_STBY	PVSS ESD VDD Standby Power	0	0	0	uW
PWR_PVSSQ_STBY	PVSSQ VDDQ Standby Power	0	0	0	uW
PWR_PVSSQ_STBY	PVSSQ ESD VDD Standby Power	0	0	0	uW

Table. 3-21: PZQ Power Specifications – DDR3L Mode (ZQ_OFF deasserted)

Symbol	Parameter	Min	Nom	Max	Units
PDR_VQ_34	VDDQ Power ZQ_OFF deasserted – drive 34	27.64	31.28	37.31	mW
PDR_VQ_40	VDDQ Power ZQ_OFF deasserted – drive 40	24.25	27.61	32.87	mW
PDR_VQ_50	VDDQ Power ZQ_OFF deasserted – drive 50	19.05	22.02	26.23	mW
PRC_VQ_40	VDDQ Power ZQ_OFF deasserted – odt 40	15.45	17.89	21.58	mW
PRC_VQ_60	VDDQ Power ZQ_OFF deasserted – odt 60	11.44	13.35	16.48	mW
PRC_VQ_120	VDDQ Power ZQ_OFF deasserted – odt 120	7.48	9.09	11.48	mW
PRCV	VDD Power ZQ_OFF deasserted	0	0.03	28.16	uW

3.4.7. SD Card I/F I/O Buffer

3.4.7.1. 3.3V Specifications

Table 3-22: SD Card I/F I/O 3.3V Specifications

Parameter	Symbol	Condition		Rating			Unit
				Min.	Typ.	Max.	
H level output voltage	VOH	2mA buffer	IOH = -2mA	VDE_SDIO[1:0] - 0.4	—	VDE_SDIO[1:0]	V
		6mA buffer	IOH = -6mA				
		10mA buffer	IOH = -10mA				
		17mA buffer	IOH = -17mA				
L level output voltage	VOL	2mA buffer	IOL = 2mA	0	—	0.4	V
		6mA buffer	IOL = 6mA				
		10mA buffer	IOL = 10mA				
		17mA buffer	IOL = 17mA				
Pull-Up resistance	Rpu	@VIL=0V	Target	10	—	90	kΩ
			Characteristics	30	41	56	
Input threshold voltage	VTH	Characteristics		0.76	0.85	0.94	V
Input leak	IL	Target		-10	—	10	uA
		Characteristics		-10	—	10	

- 3.3V Specifications V - I CHARACTERISTICS (2mA buffer)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE_SDIO[1:0] = 3.0 V
	TYP: Process = Typical	T_J = 25°C	VDE_SDIO[1:0] = 3.3 V
	MAX: Process = Fast	T_J = 0°C	VDE_SDIO[1:0] = 3.45 V

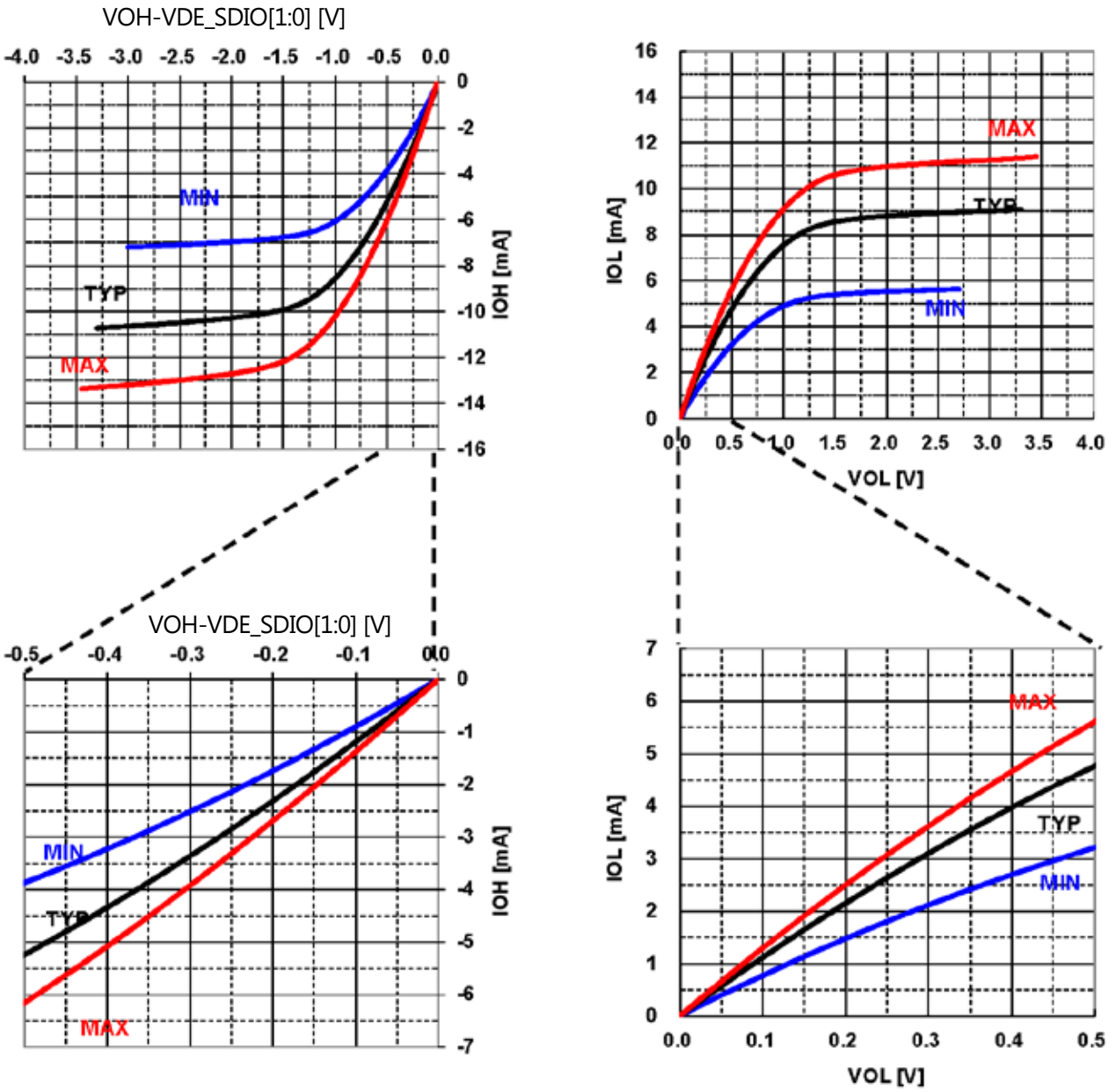


Figure 3-9: 3.3V Specifications V - I CHARACTERISTICS (2mA buffer)

- 3.3V Specifications V - I CHARACTERISTICS (6mA buffer)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE_SDIO[1:0] = 3.0 V
	TYP: Process = Typical	T_J = 25°C	VDE_SDIO[1:0] = 3.3 V
	MAX: Process = Fast	T_J = 0°C	VDE_SDIO[1:0] = 3.45 V

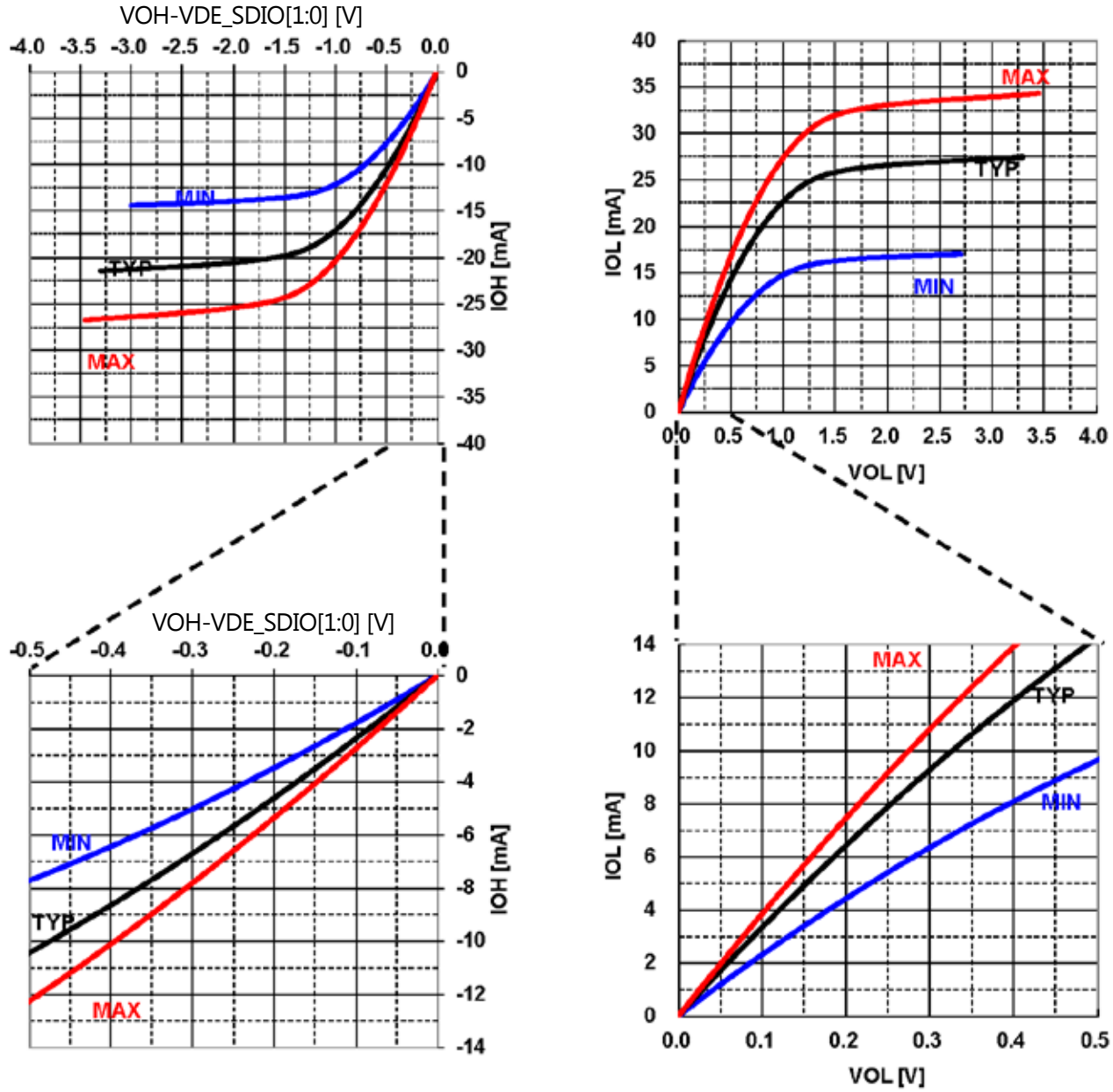


Figure 3-10: 3.3V Specifications V - I CHARACTERISTICS (6mA buffer)

- 3.3V Specifications V - I CHARACTERISTICS (10mA buffer)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE_SDIO[1:0] = 3.0 V
	TYP: Process = Typical	T_J = 25°C	VDE_SDIO[1:0] = 3.3 V
	MAX: Process = Fast	T_J = 0°C	VDE_SDIO[1:0] = 3.45 V

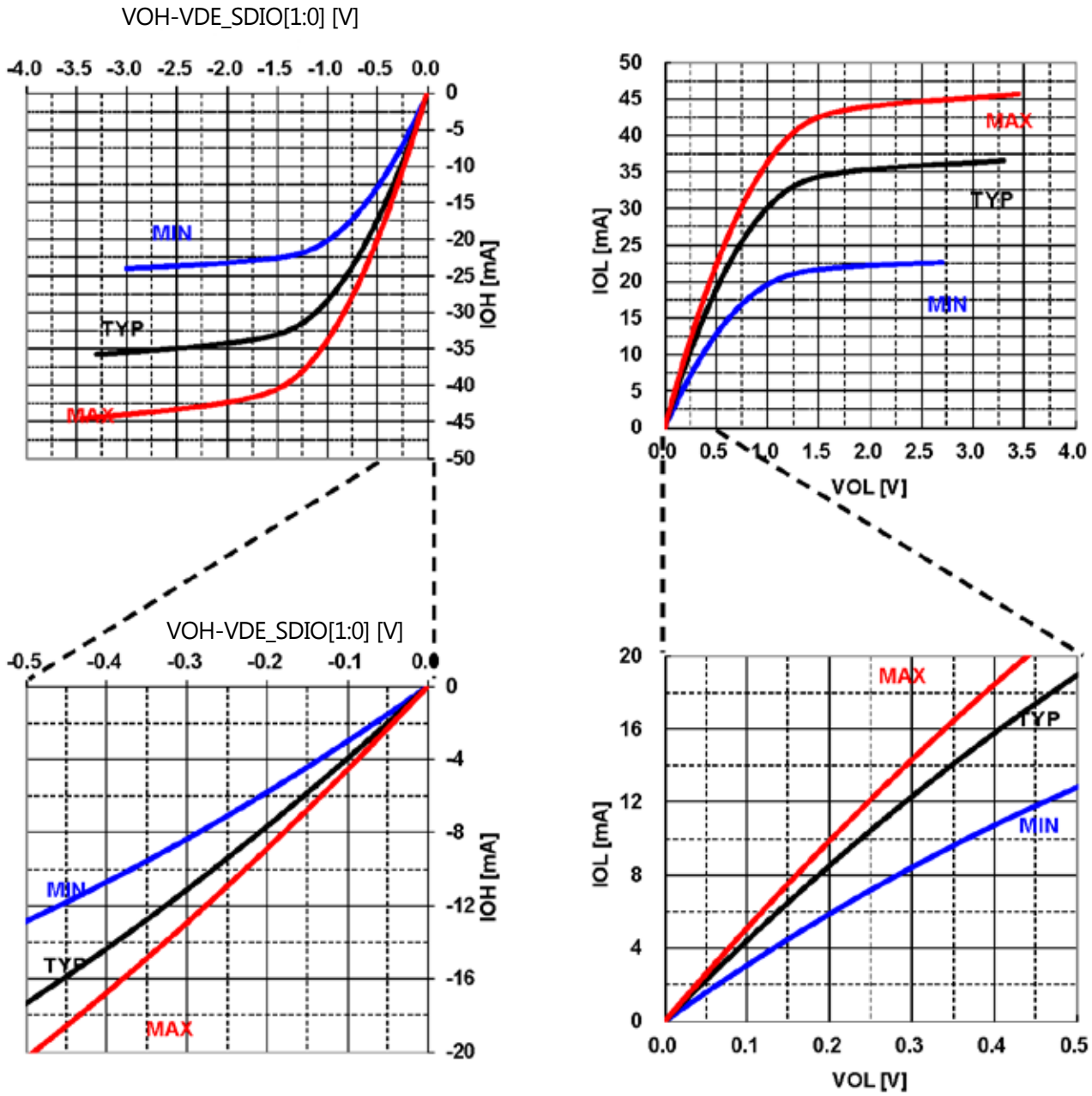


Figure 3-11: 3.3V Specifications V - I CHARACTERISTICS (10mA buffer)

- 3.3V Specifications V - I CHARACTERISTICS (17mA buffer)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE_SDIO[1:0] = 3.0 V
	TYP: Process = Typical	T_J = 25°C	VDE_SDIO[1:0] = 3.3 V
	MAX: Process = Fast	T_J = 0°C	VDE_SDIO[1:0] = 3.45 V

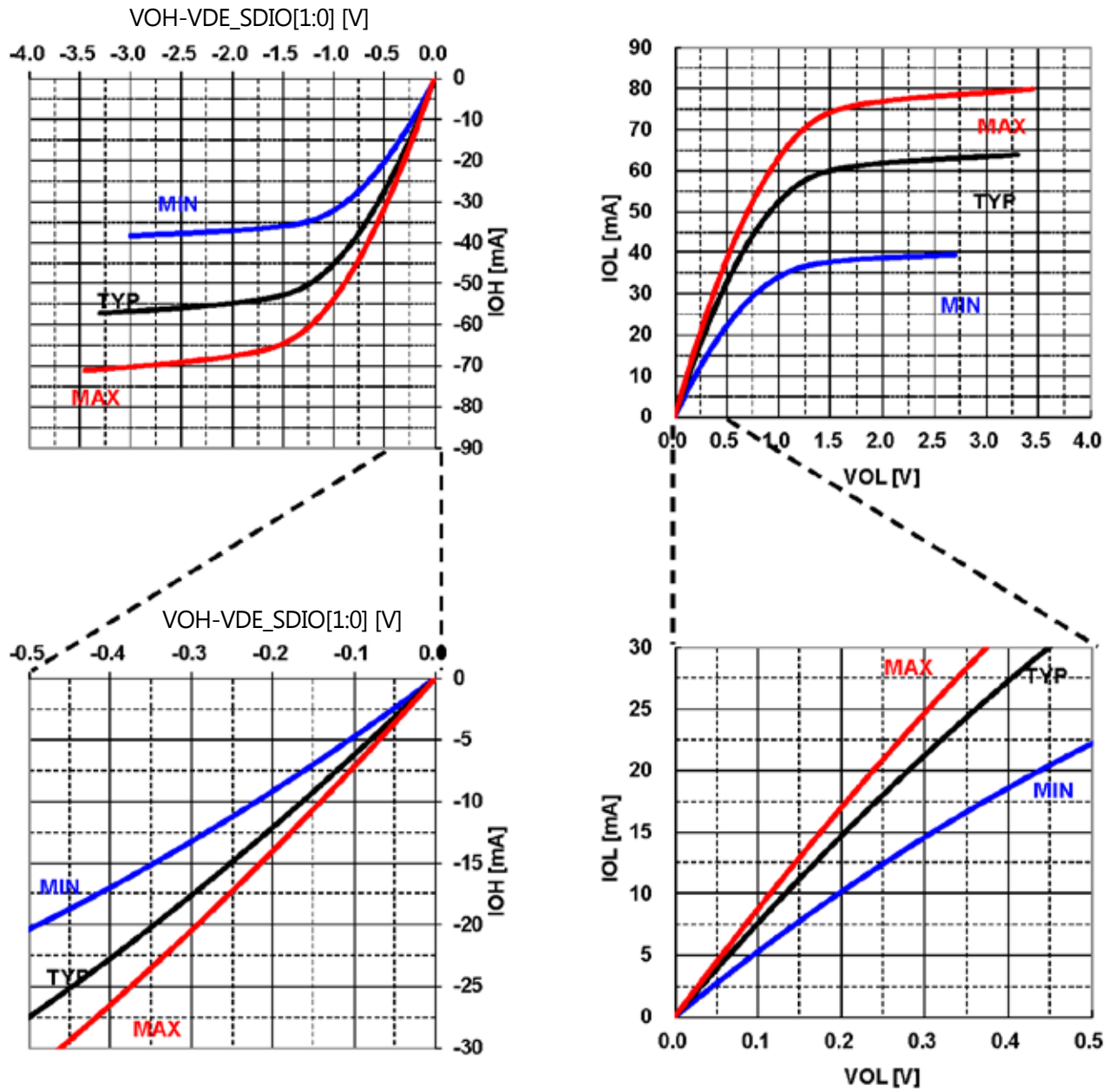


Figure 3-12: 3.3V Specifications V - I CHARACTERISTICS (17mA buffer)

3.4.7.2. 1.8V Specifications

Table 3-23: SD Card I/F I/O 1.8V Specifications

Parameter	Symbol	Condition		Rating			Unit
				Min.	Typ.	Max.	
H level output voltage	VOH	IOH = -2mA		VDE_SDIO[1:0] - 0.4	—	VDE_SDIO[1:0]	V
L level output voltage	VOL	IOL = 2mA		0	—	0.4	V
Output impedance	Ron	Driver Type A	Target	—	33	—	Ω
			Characteristics	17	24	40	
		Driver Type B	Target	—	50	—	
			Characteristics	22	35	57	
		Driver Type C	Target	—	66	—	
			Characteristics	25	41	68	
		Driver Type D	Target	—	100	—	
			Characteristics	44	67	108	
Pull-Up resistance	Rpu	@VIL=0V	Target	10	—	90	kΩ
			Characteristics	29	40	54	
Input threshold voltage	VTH	Characteristics		0.81	0.90	1.13	V
Input leak	IL	Target		-2	—	2	uA
		Characteristics		-2	—	2	

- 1.8V Specifications V - I CHARACTERISTICS (Type A)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE_SDIO[1:0] = 1.70 V
	TYP: Process = Typical	T_J = 25°C	VDE_SDIO[1:0] = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE_SDIO[1:0] = 1.95 V

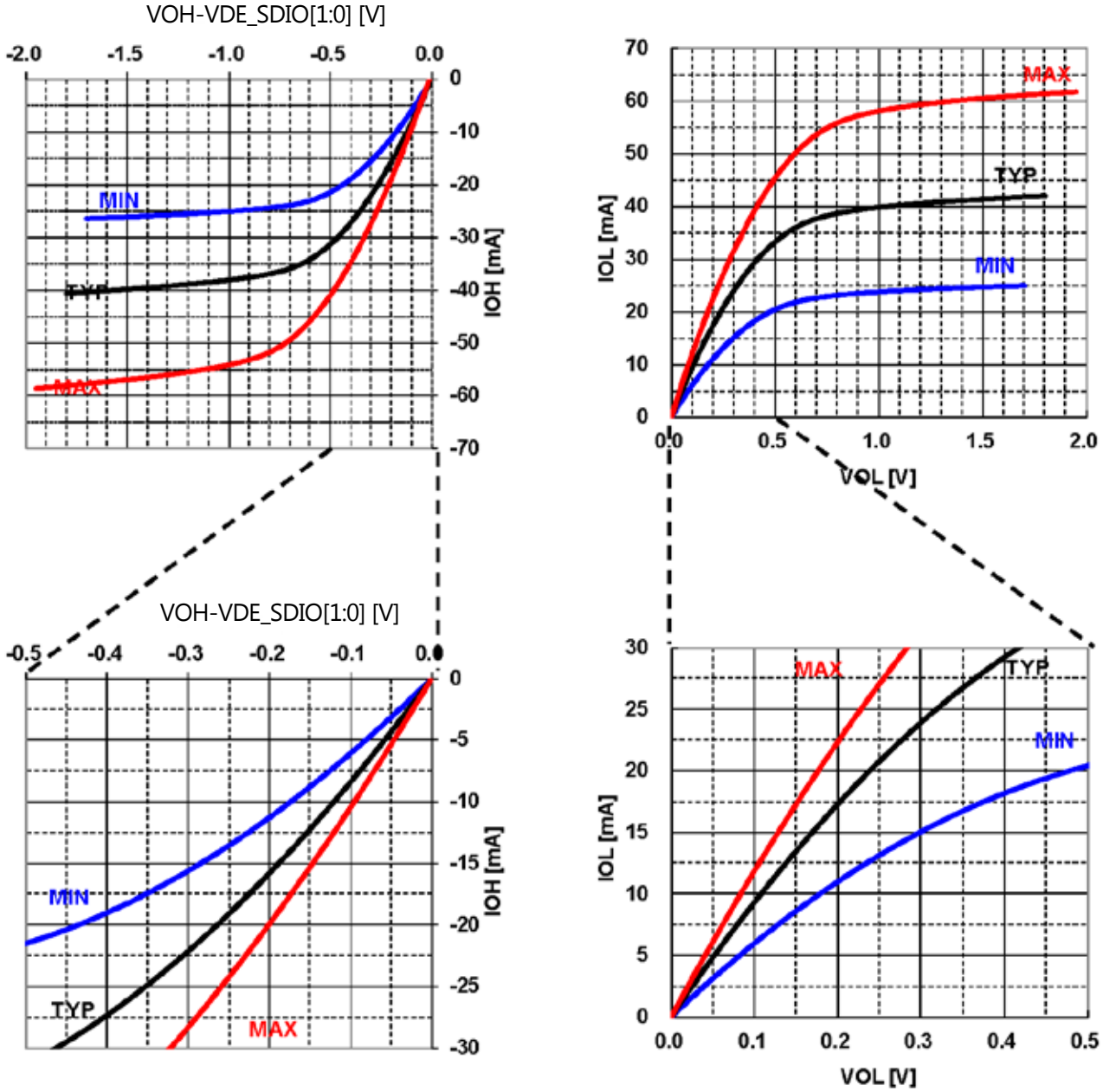


Figure 3-13: 1.8V Specifications V - I CHARACTERISTICS (Type A)

- 1.8V Specifications V - I CHARACTERISTICS (Type B)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE_SDIO[1:0] = 1.70 V
	TYP: Process = Typical	T_J = 25°C	VDE_SDIO[1:0] = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE_SDIO[1:0] = 1.95 V

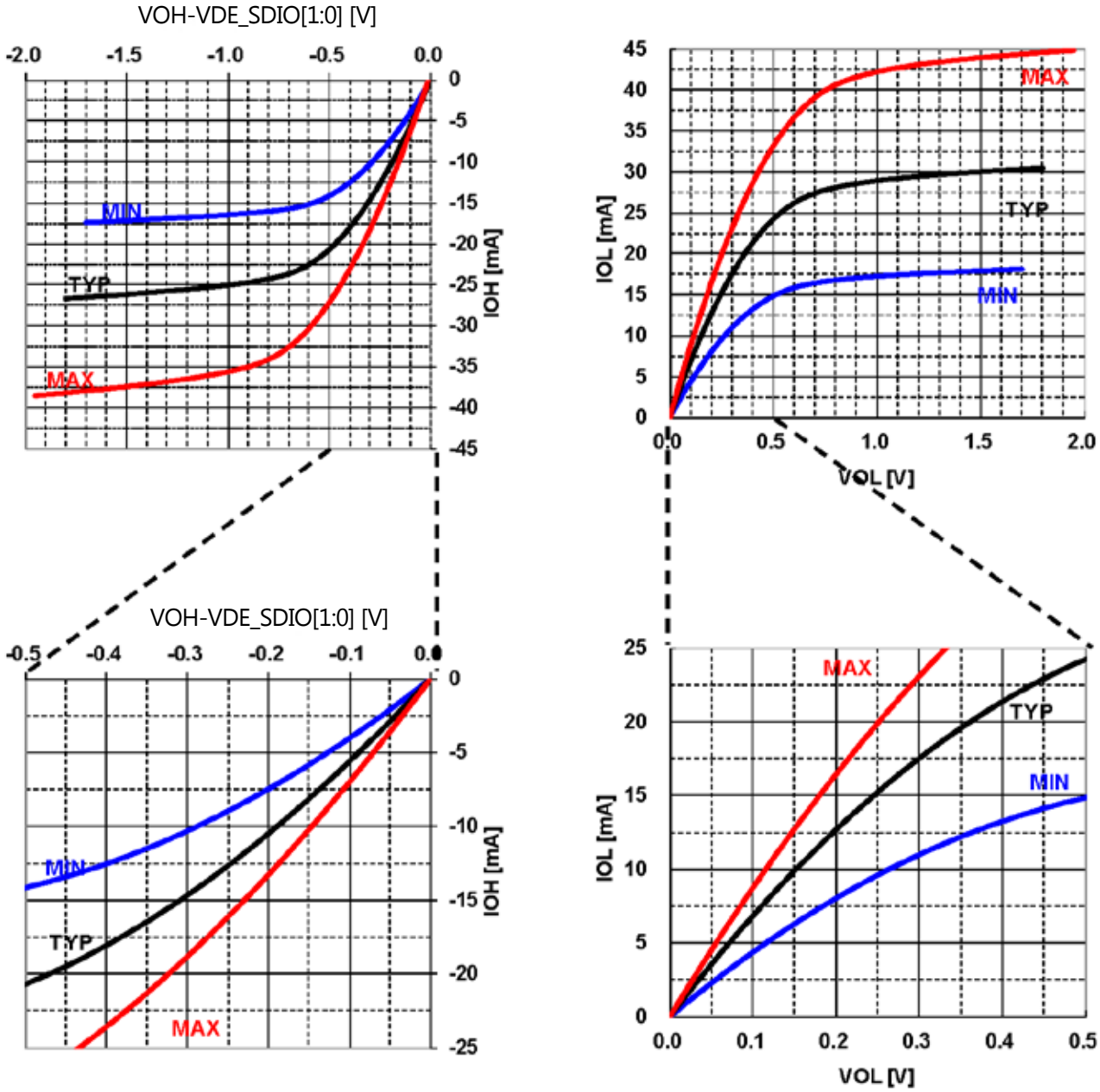


Figure 3-14: 1.8V Specifications V - I CHARACTERISTICS (Type B)

- 1.8V Specifications V - I CHARACTERISTICS (Type C)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE_SDIO[1:0] = 1.70 V
	TYP: Process = Typical	T_J = 25°C	VDE_SDIO[1:0] = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE_SDIO[1:0] = 1.95 V

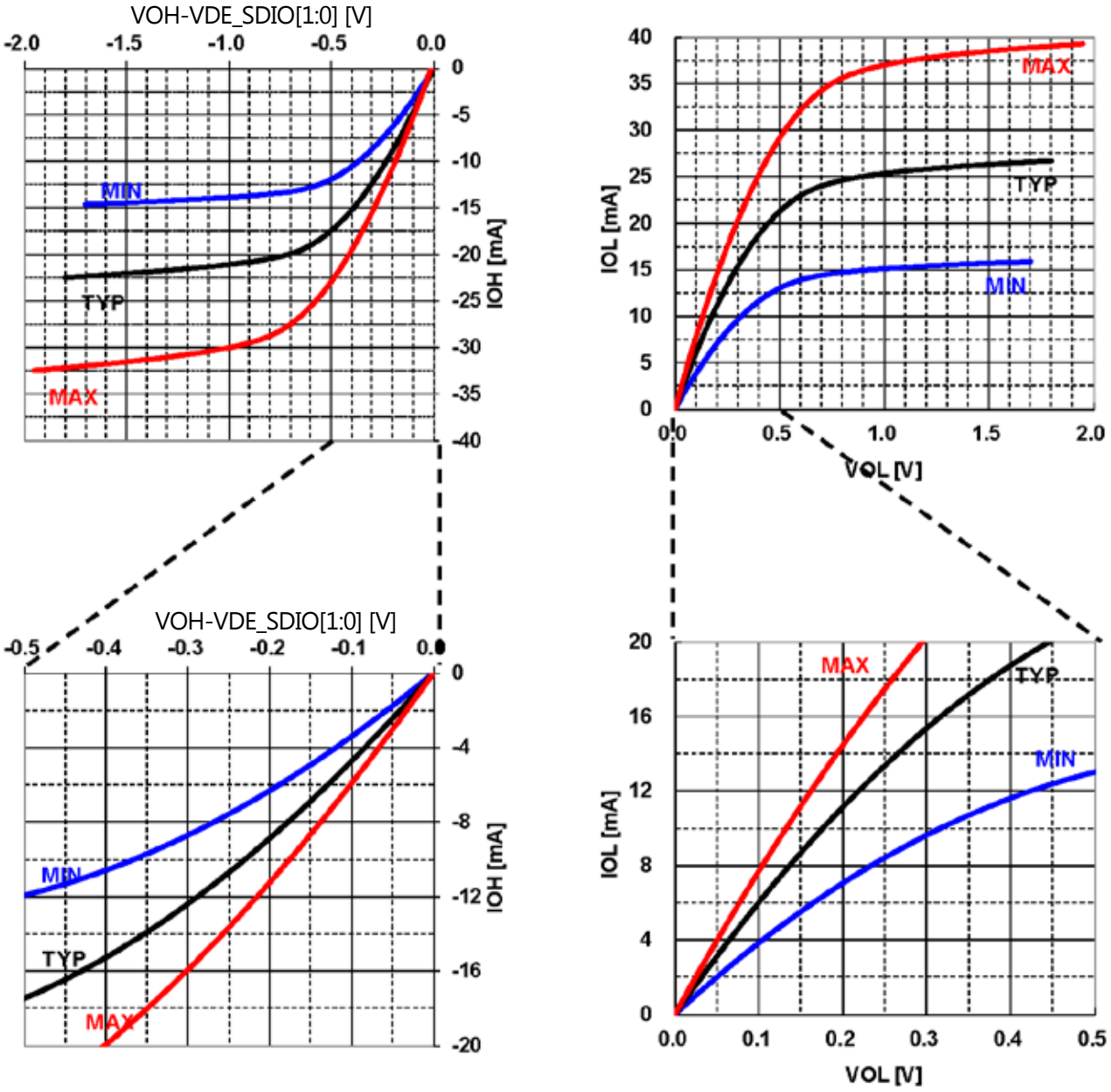


Figure 3-15: 1.8V Specifications V - I CHARACTERISTICS (Type C)

- 1.8V Specifications V - I CHARACTERISTICS (Type D)

Conditions	MIN: Process = Slow	T_J = 110°C	VDE_SDIO[1:0] = 1.70 V
	TYP: Process = Typical T_J = 25°C		VDE_SDIO[1:0] = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE_SDIO[1:0] = 1.95 V

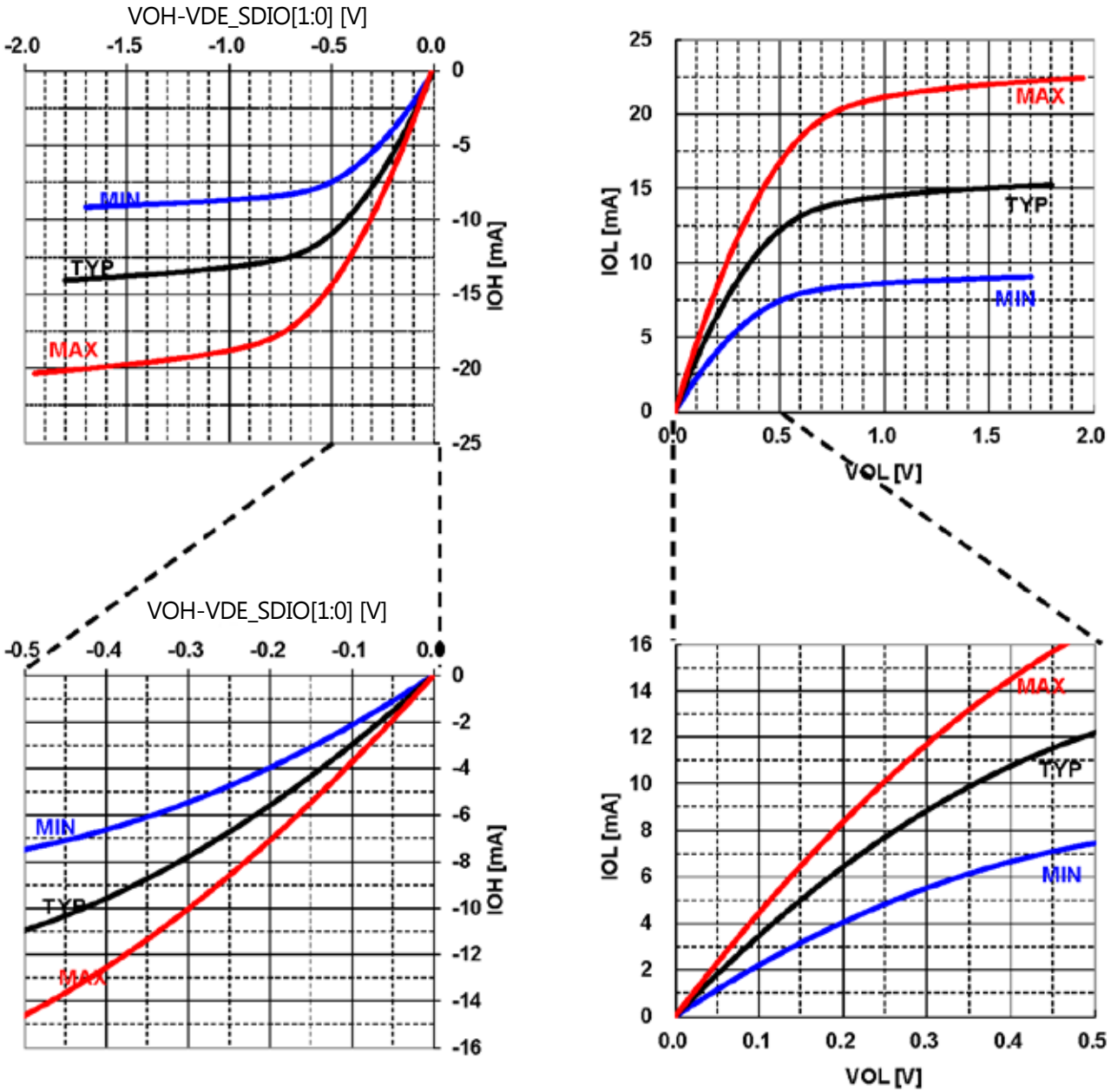


Figure 3-16: 1.8V Specifications V - I CHARACTERISTICS (Type D)

3.4.8. eMMC4.51 HS200(1.8V) I/O Buffer

Table 3-24: eMMC4.51 HS200 (1.8V) I/O Specifications

Parameter	Symbol	Condition (*4)		Rating			Unit
				Min.	Typ.	Max.	
H level output voltage	VOH	IOH = -2mA		VDE - 0.45	—	—	V
L level output voltage	VOL	IOL = 2mA		—	—	0.45	V
Output impedance (*1)	Ron	Driver Type 0	Target	—	50	—	Ω
			Characteristics	36	45	60	
		Driver Type 1	Target	—	33	—	
			Characteristics	29	36	46	
		Driver Type 2	Target	—	66	—	
			Characteristics	43	55	74	
		Driver Type 3	Target	—	100	—	
			Characteristics	80	102	145	
Input leak (*2)	IL	Target		-2.0	—	2.0	uA
		Characteristics		-1.0	—	1.0	
Pull-Up resistance (*3)	Rpu	Target		4.7	—	50.0	kΩ
		Characteristics		19.0	25.0	35.0	

(*1) : Calculated from the output current when the output voltage is 0.9V.
(*2) : The current when the input voltage VIL=0V and VIH=VDDE. Pull-Up resistance is OFF.
(*3) : The resistance value when the input voltage VIL=0V.
(*4) : "Target": Extracted from eMMC standards document. "Characteristics": This I/O cell characteristics.

- Driver Type-0 [Ron:50Ω] Output V - I CHARACTERISTICS

Conditions	MIN: Process = Slow	T_J = 110°C	VDE = 1.70 V
	TYP: Process = Typical	T_J = 25°C	VDE = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE = 1.95 V

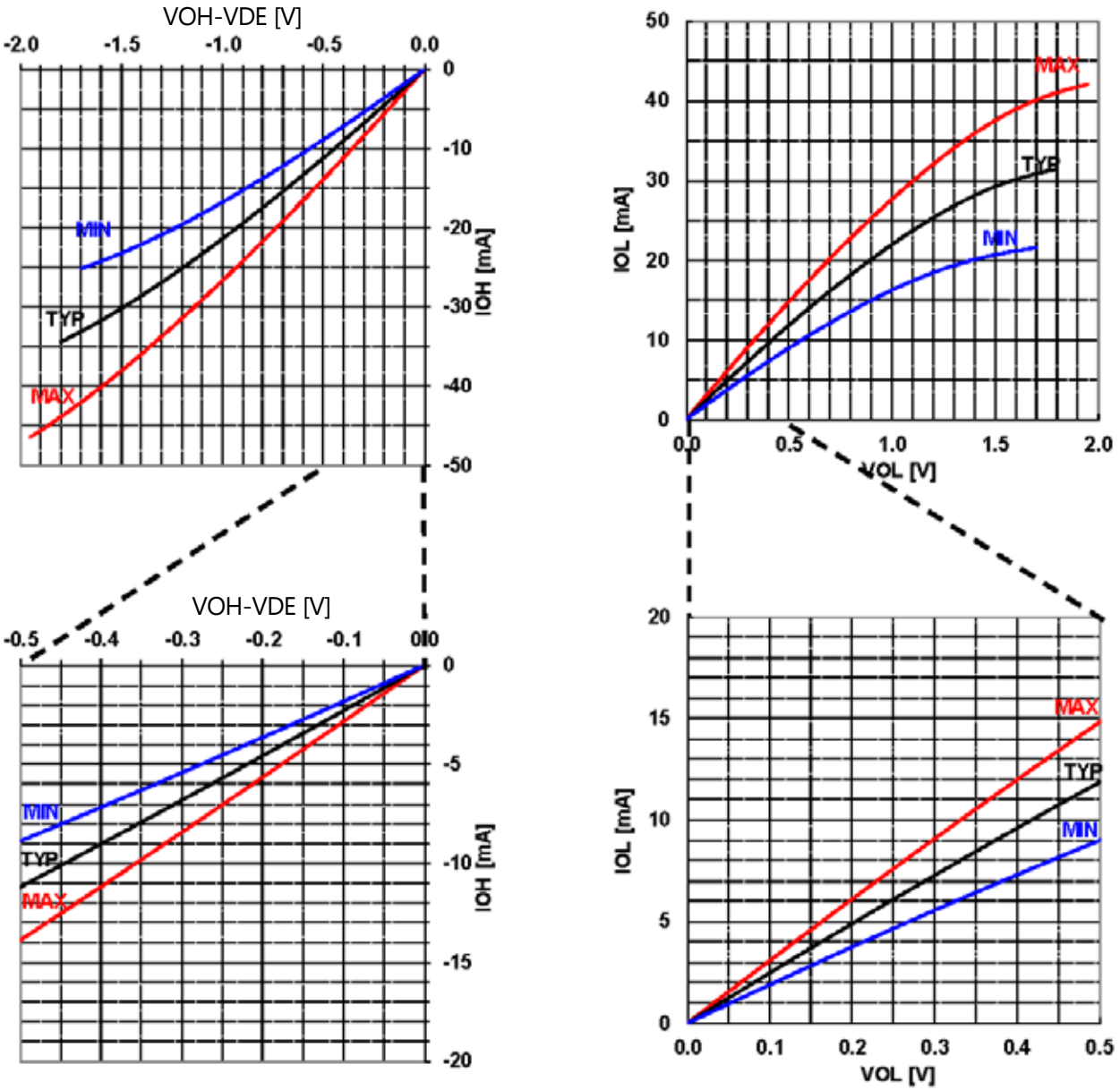


Figure 3-17: Driver Type-0 [Ron:50Ω] Output V - I CHARACTERISTICS

- Driver Type-0 [Ron:33Ω] Output V - I CHARACTERISTICS

Conditions	MIN: Process = Slow	T_J = 110°C	VDE = 1.70 V
	TYP: Process = Typical	T_J = 25°C	VDE = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE = 1.95 V

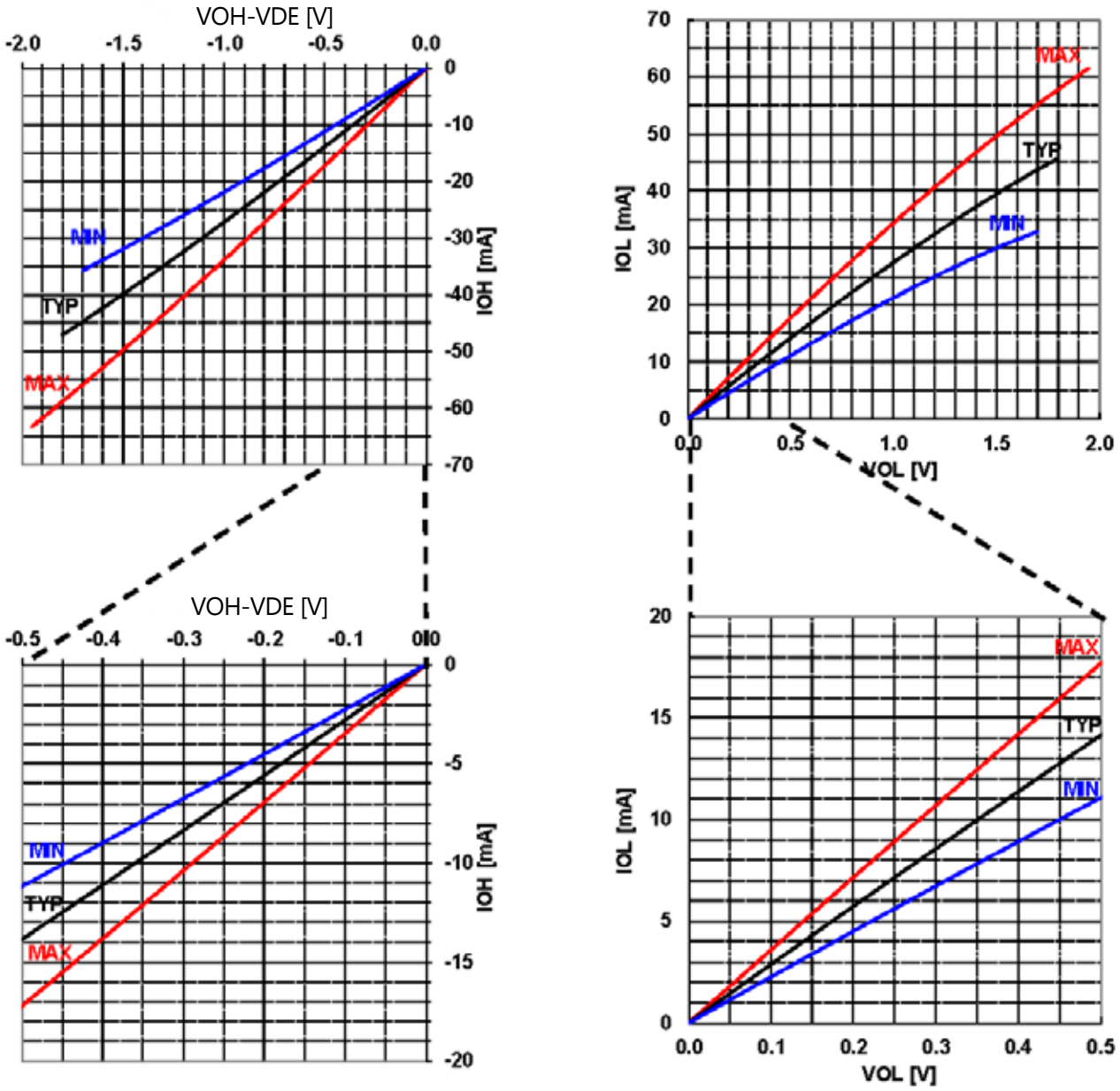


Figure 3-18: Driver Type-1 [Ron:33Ω] Output V - I CHARACTERISTICS

- Driver Type-2 [Ron:66Ω] Output V - I CHARACTERISTICS

Conditions	MIN: Process = Slow	T_J = 110°C	VDE = 1.70 V
	TYP: Process = Typical	T_J = 25°C	VDE = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE = 1.95 V

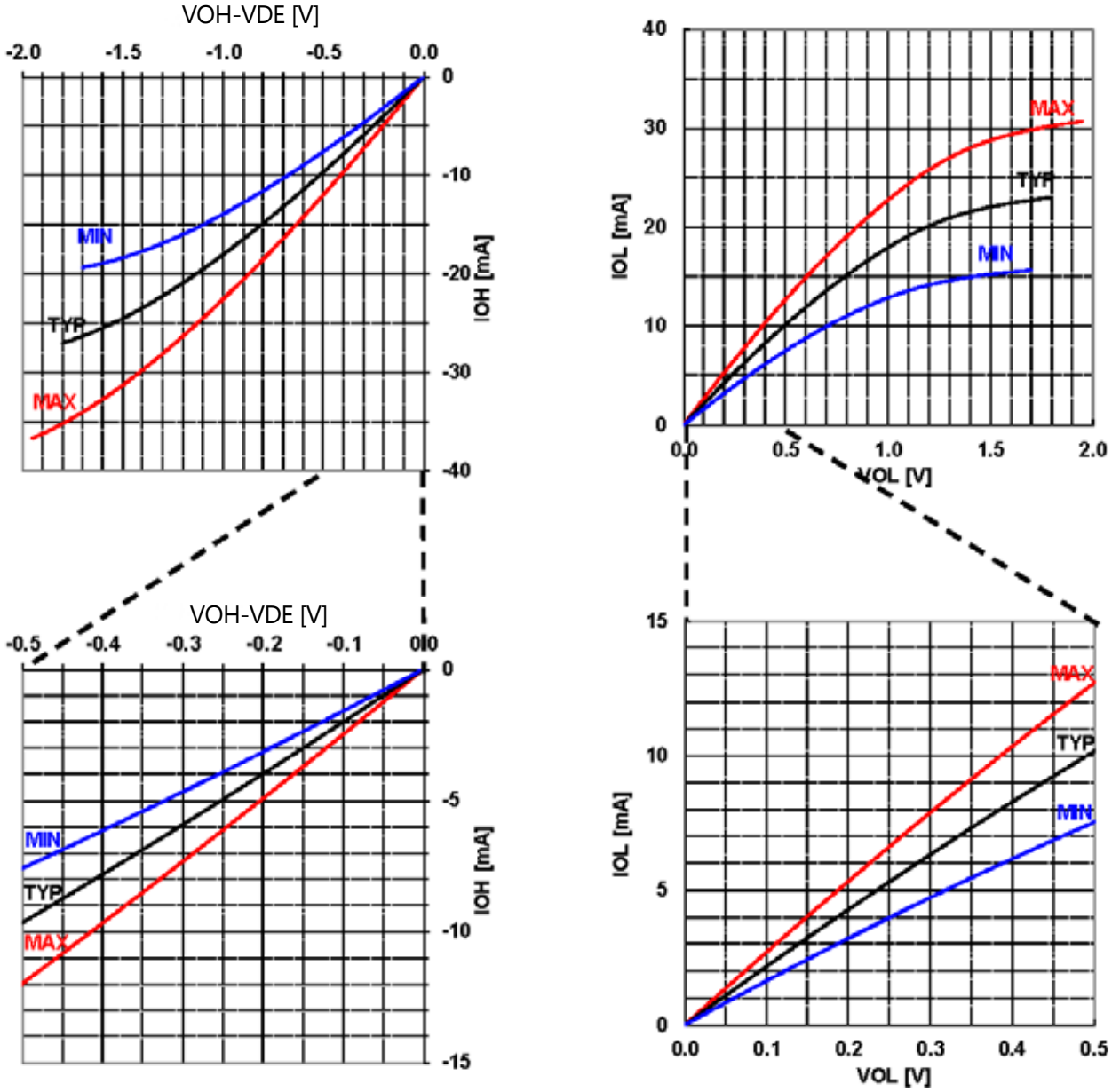


Figure 3-19: Driver Type-2 [Ron:66Ω] Output V - I CHARACTERISTICS

- Driver Type-3 [Ron:100Ω] Output V - I CHARACTERISTICS

Conditions	MIN: Process = Slow	T_J = 110°C	VDE = 1.70 V
	TYP: Process = Typical	T_J = 25°C	VDE = 1.80 V
	MAX: Process = Fast	T_J = 0°C	VDE = 1.95 V

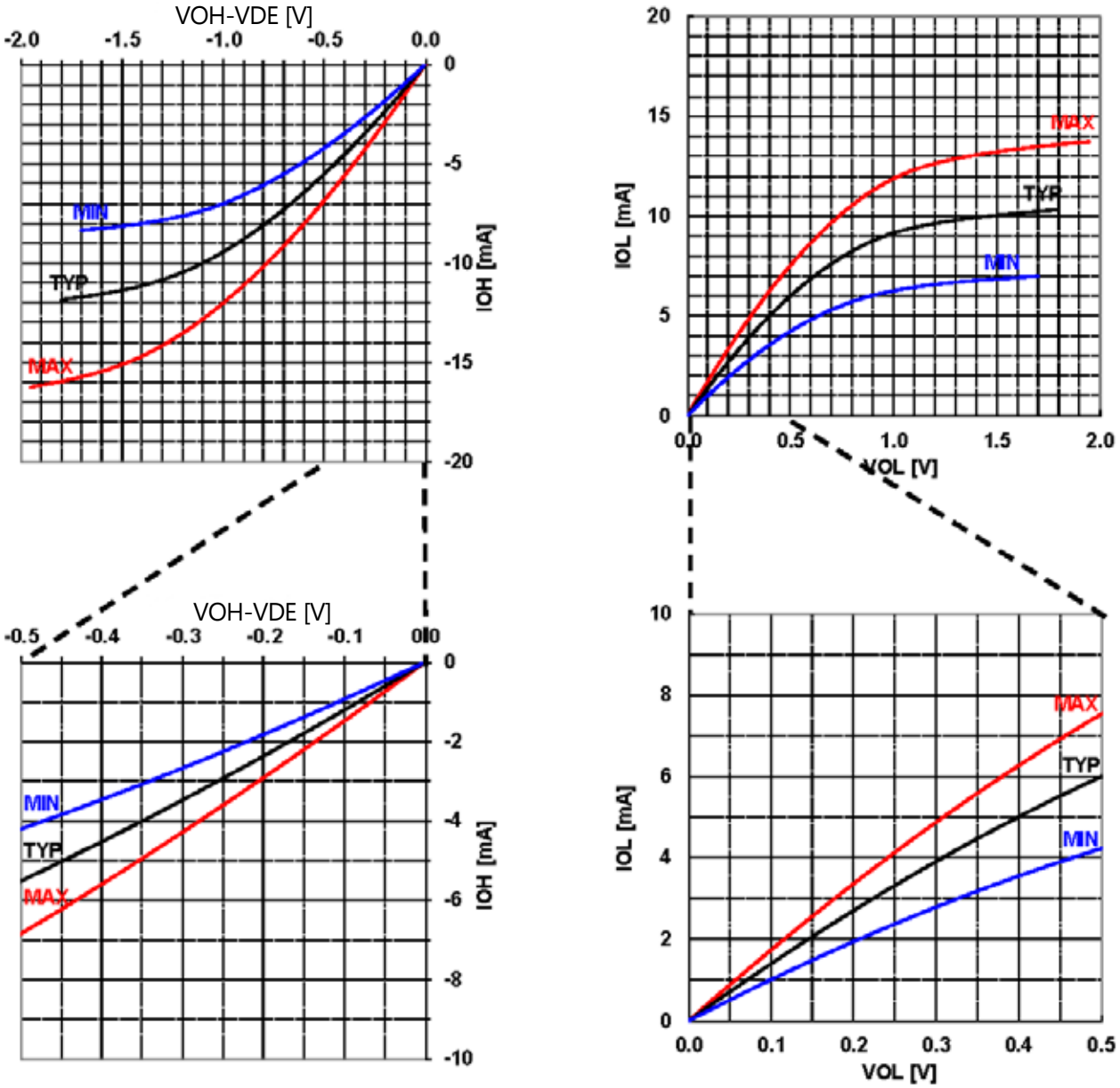


Figure 3-20: Driver Type-3 [Ron:100Ω] Output V - I CHARACTERISTICS

3.5. AC Characteristics

The AC timings of the external terminals are given in this Section.

3.5.1. JTAG Signal Timing

3.5.1.1. Input Signal

Table. 3-25: JTAG Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
TDI	t_{ISTDI}	TDI Input setup time	30			ns
	t_{IHTDI}	TDI Input hold time	0.09			ns
TMS	t_{ISTMS}	TMS Input setup time	30			ns
	t_{IHTMS}	TMS Input hold time	0.09			ns

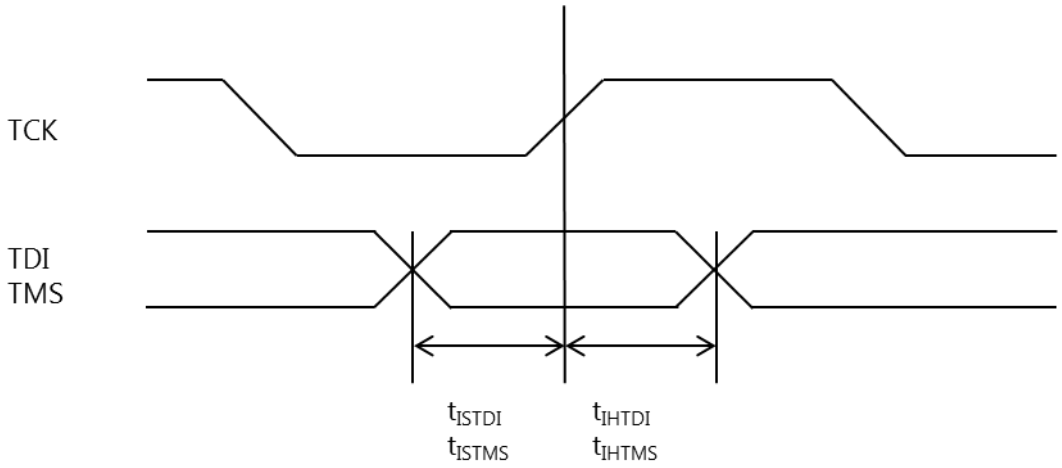


Figure. 3-21: JTAG Input Signal Timing

3.5.1.2. Output Signal

Table. 3-26: JTAG Output Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
TDO	$t_{ODLYTDO}$	TDO Output delay time	0.09		20	ns

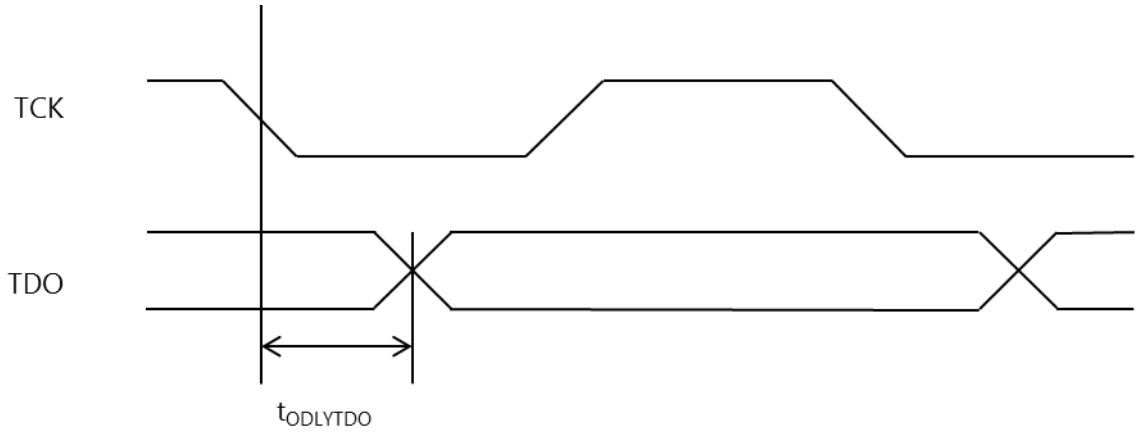


Figure. 3-22: JTAG Output Signal Timing

3.5.2. HSSPI Signal Timing

3.5.2.1. Clock

Table. 3-27: HSSPI Clock

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
HSSPI_CLK	t_{OCYC}	HSSPI_CLK cycle(*1)	10			ns
		HSSPI_CLK cycle(*2)	16			ns
		HSSPI_CLK cycle(*3)	20			ns
	t_{OWH}	HSSPI_CLK H width(*1)	4.5			ns
		HSSPI_CLK H width(*2)	7.2			ns
		HSSPI_CLK H width(*3)	9			ns
	t_{OWL}	HSSPI_CLK L width(*1)	4.5			ns
		HSSPI_CLK L width(*2)	7.2			ns
		HSSPI_CLK L width(*3)	9			ns

(*1) : 100MHz (Clock selection PCLK 1/1 frequency division ratio)
(*2) : 62.5MHz (Clock selection HCLK 1/2 frequency division ratio)
(*3) : 50MHz (Clock selection PCLK 1/2 frequency division ratio)

3.5.2.2. Input Signal

Table. 3-28: HSSPI Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
HSSPI_DAT[3:0]	t_{ISDAT}	HSSPI_DAT Input setup time(*1)	1.2			ns
		HSSPI_DAT Input setup time(*2)	0.7			ns
		HSSPI_DAT Input setup time(*3)	4.7			ns
	t_{IHDAT}	HSSPI_DAT Input hold time(*1)	0			ns
		HSSPI_DAT Input hold time(*2)	0			ns
		HSSPI_DAT Input hold time(*3)	0			ns

(*1) : 100MHz (Clock selection PCLK 1/1 frequency division ratio)
(*2) : 62.5MHz (Clock selection HCLK 1/2 frequency division ratio)
(*3) : 50MHz (Clock selection PCLK 1/2 frequency division ratio)

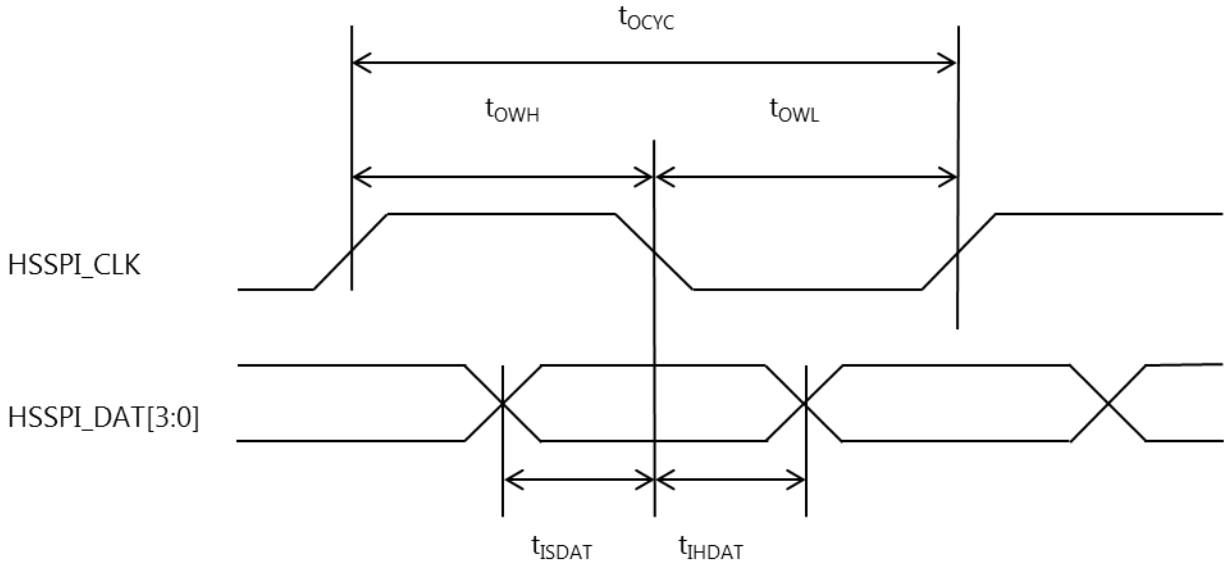


Figure. 3-23: HSSPI Input Signal Timing

3.5.2.3. Output Signal

Table. 3-29: HSSPI Output Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
HSSPI_DAT[3:0]	$t_{ODLYDAT}$	HSSPI_DAT Output delay time(*1)	0.4		1.6	ns
		HSSPI_DAT Output delay time(*2)	-3.6		2.6	ns
		HSSPI_DAT Output delay time(*3)	-4.6		4.6	ns
HSSPI_CSO[1:0]	$t_{ODLYCSO}$	HSSPI_CSO Output delay time(*1)	-14.6		4.6	ns
		HSSPI_CSO Output delay time(*2)	-26.6		5.6	ns
		HSSPI_CSO Output delay time(*3)	-27.6		14.6	ns

(*1) : 100MHz (Clock selection PCLK 1/1 frequency division ratio)
(*2) : 62.5MHz (Clock selection HCLK 1/2 frequency division ratio)
(*3) : 50MHz (Clock selection PCLK 1/2 frequency division ratio)

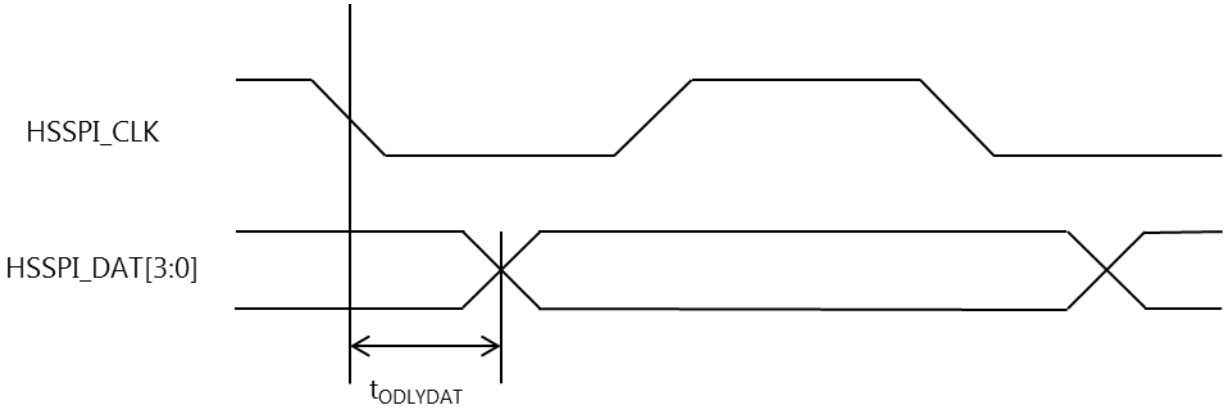


Figure. 3-24: HSSPI Output Signal Timing

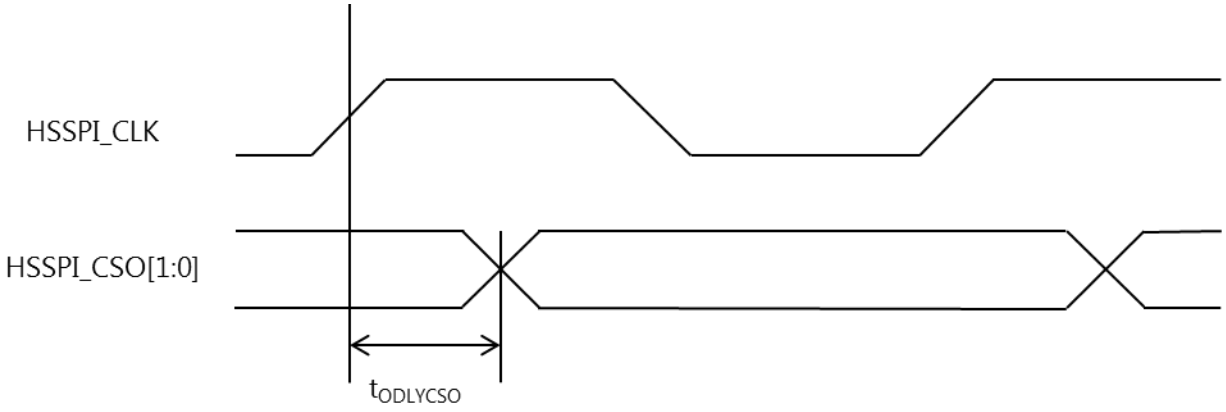


Figure. 3-25: HSSPI Output Signal Timing

3.5.3. e･MMC Signal Timing

3.5.3.1. Clock

Table. 3-30: e･MMC Clock

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
EMMC_CLK	t_{OWH}	EMMC_CLK H width (HS200)	1.5			ns
	t_{OWL}	EMMC_CLK L width (HS200)	1.5			ns
	t_{OWH}	EMMC_CLK H width (Backward, High, DDR)	9			ns
	t_{OWL}	EMMC_CLK L width (Backward, High, DDR)	9			ns

3.5.3.2. Input Signal

Table. 3-31: e･MMC Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
EMMC_DAT[7:0]	t_{ISDAT}	EMMC_DAT Input setup time (Backward, High, DDR)	2.2			ns
	t_{IHDAT}	EMMC_DAT Input hold time (Backward, High, DDR)	1.5			ns
EMMC_CMD	t_{ISCMD}	EMMC_CMD Input setup time (Backward, High, DDR)	5.5			ns
	t_{IHCMD}	EMMC_CMD Input hold time (Backward, High, DDR)	2.5			ns

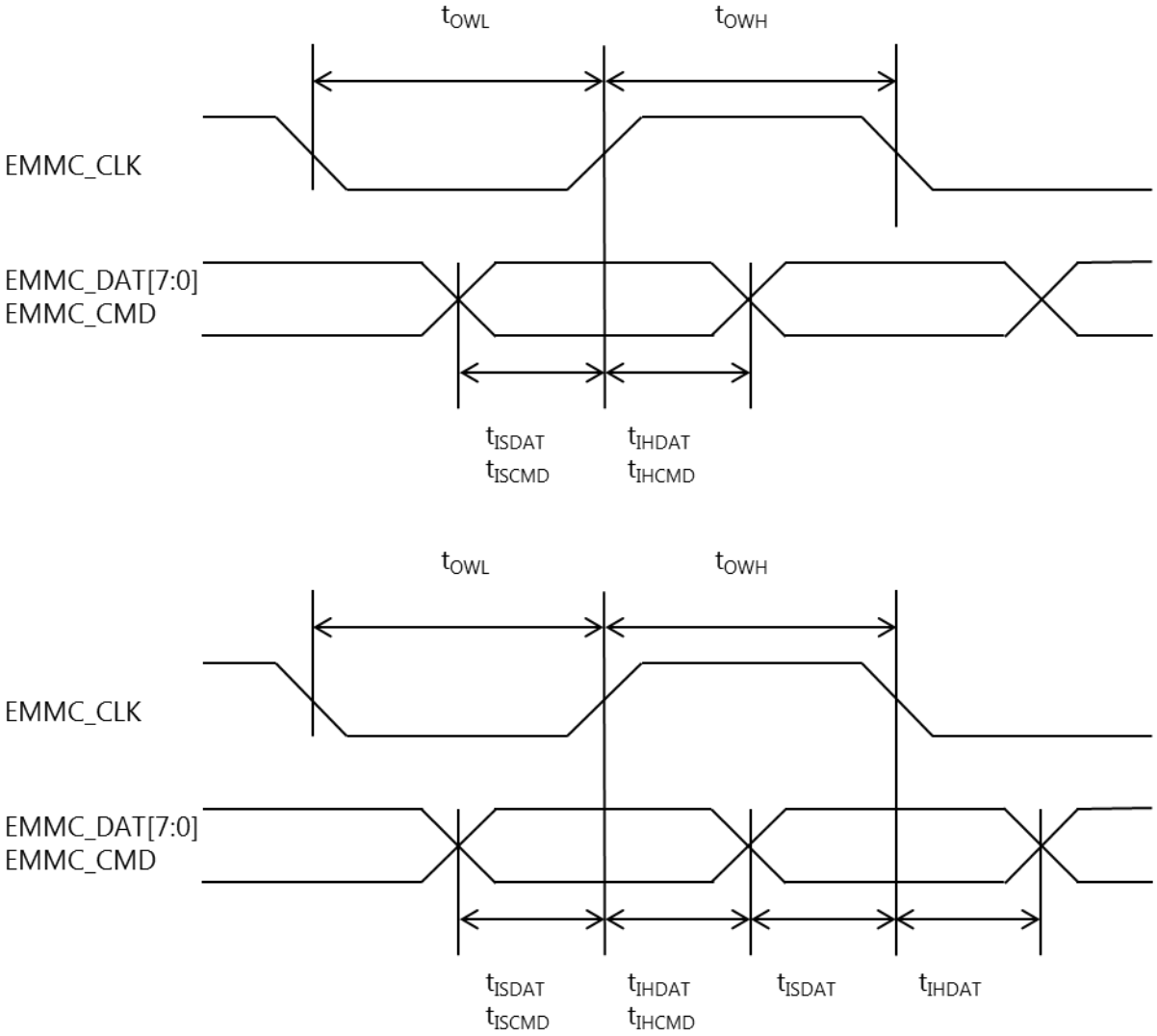


Figure. 3-26: e·MMC Input Signal Timing

3.5.3.3. Output Signal

Table. 3-32: e･MMC Output Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
EMMC_DAT[7:0] EMMC_CMD	$t_{ODLYDAT1}$	EMMC_DAT Output delay time (Backward, High) *1	3.4		6.6	ns
	$t_{ODLYCMD1}$	EMMC_CMD Output delay time (Backward, High)*1	3.4		6.6	ns
	$t_{ODLYDAT2}$	EMMC_DAT Output delay time (DDR)*1	3.4		6.6	ns
	$t_{ODLYCMD2}$	EMMC_CMD Output delay time (DDR)*1	3.4		6.6	ns
	$t_{ODLYDAT3}$	EMMC_DAT Output delay time (HS200)*2	1.2		3.2	ns
	$t_{ODLYCMD3}$	EMMC_CMD Output delay time (HS200)*2	1.2		3.2	ns

*1 : Division mode, Hold time care.
*2 : Non division mode, No HOLD time care.

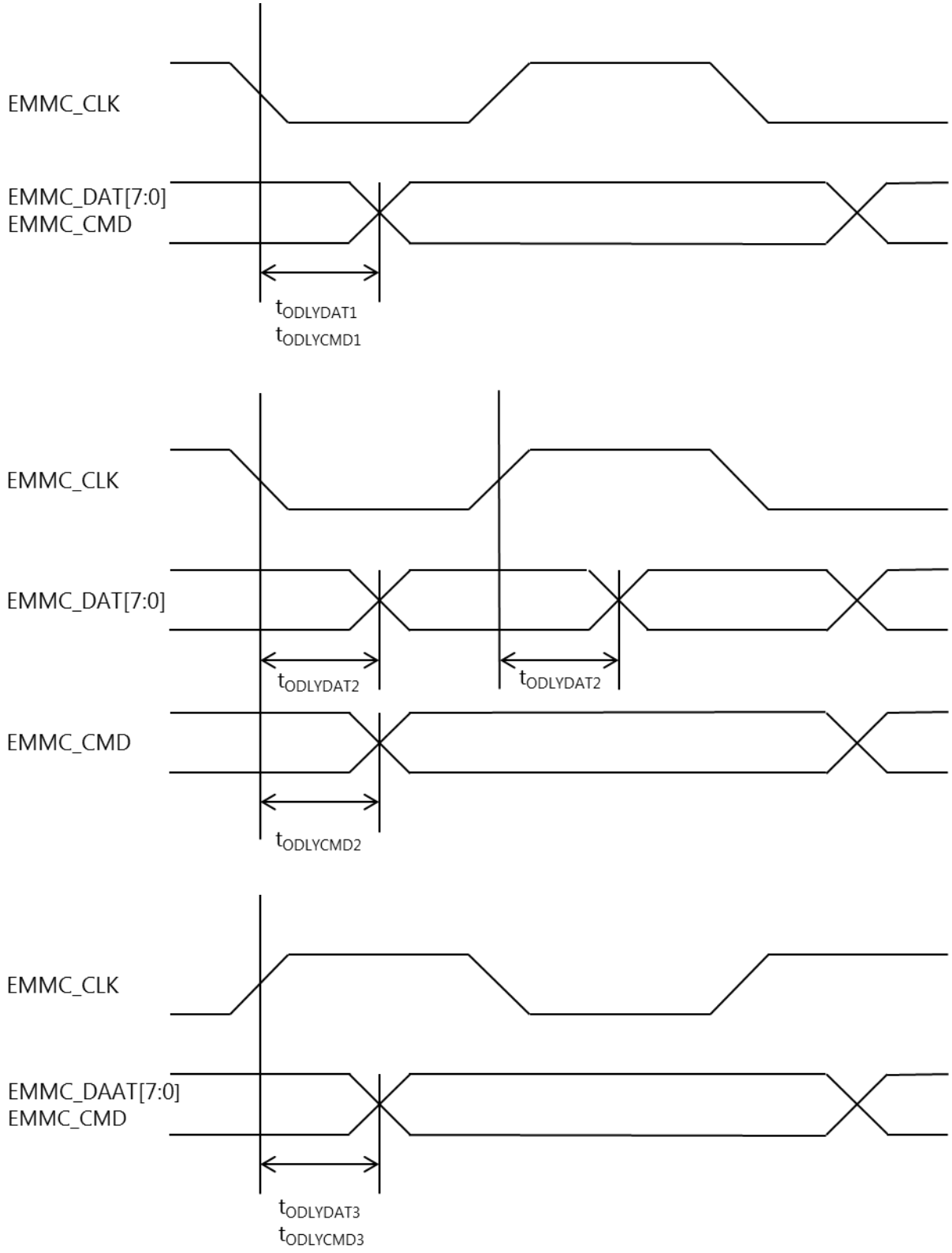


Figure. 3-27: e･MMC Output Signal Timing

3.5.4. NAND Signal Timing

3.5.4.1. Input Signal

Table. 3-33: NAND Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
PD[23:8] (NANDD[15:0])	t_{ISD}	NANDD Input setup time	20			ns
	t_{IHD}	NANDD Input hold time	2.4			ns
PD26 (NANDBUSY)	t_{ISBUSY}	NANDBUSY Input setup time	20			ns
	t_{IHBUSY}	NANDBUSY Input hold time	2.4			ns

The reference clock is the internal clock.

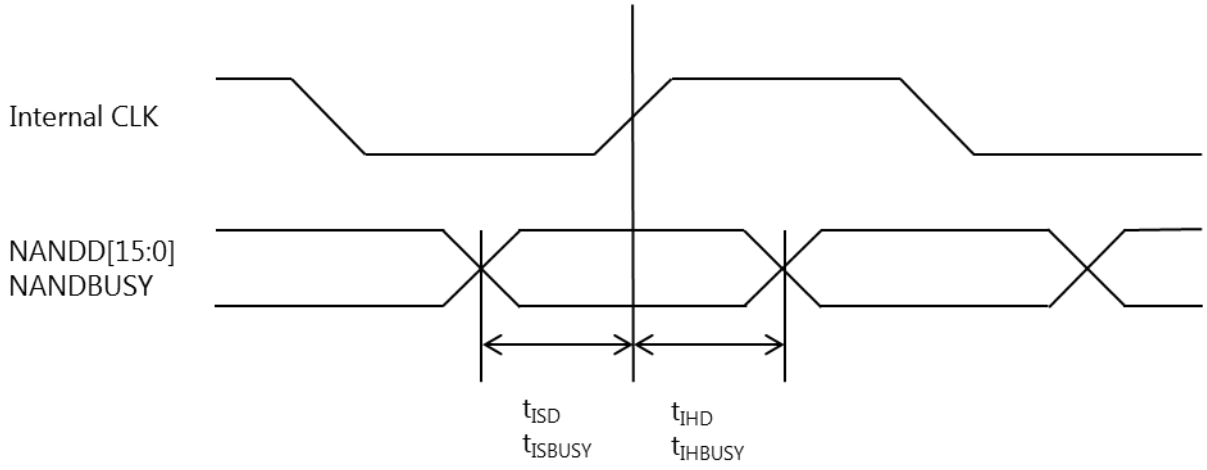


Figure. 3-28: NAND Input Signal Timing

3.5.4.2. Output Signal

Table. 3-34: NAND Output Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
PD[23:8] (NANDD[15:0])	t_{ODLYD}	NANDD Output delay time	0		22.4	ns
PD[25:24] (NANDCS[1:0])	t_{ODLYCS}	NANDCS Output delay time	0		22.4	ns
PD27 (NANDALE)	$t_{ODLYALE}$	NANDALE Output delay time	0		22.4	ns
PD28 (NANDCLE)	$t_{ODLYCLE}$	NANDCLE Output delay time	0		22.4	ns
PD29 (NANDWE)	t_{ODLYWE}	NANDWE Output delay time	0		22.4	ns
PD30 (NANDRE)	t_{ODLYRE}	NANDRE Output delay time	0		22.4	ns

The reference clock of output delay is the internal clock.

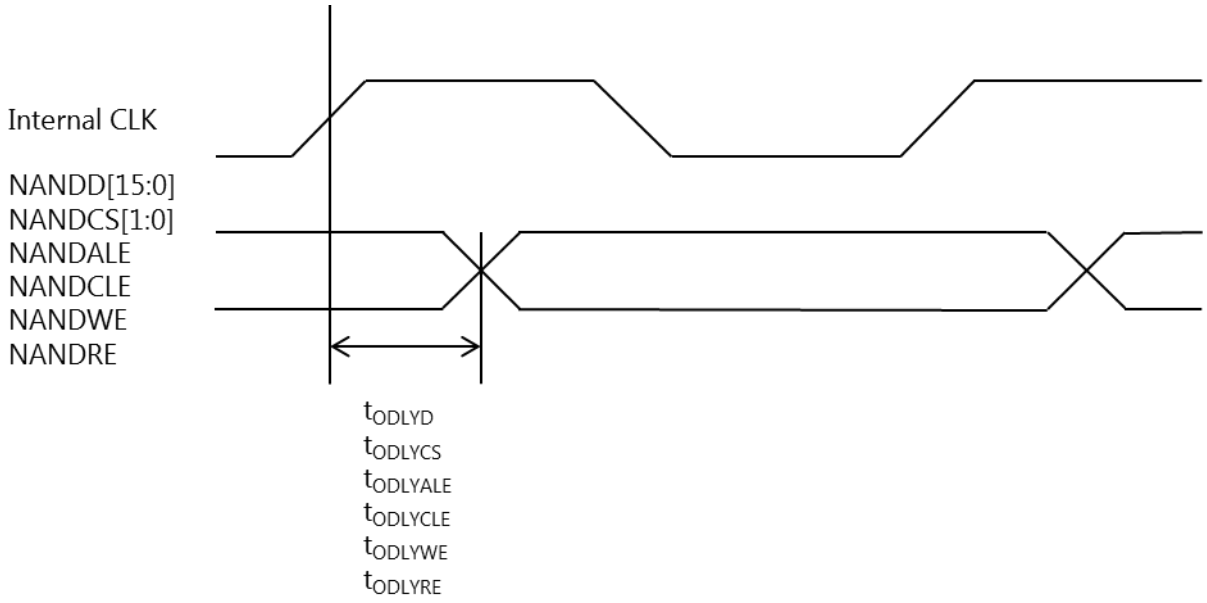


Figure. 3-29: NAND Output Signal Timing

3.5.5. MEMCS Signal Timing

3.5.5.1. Input Signal

Table. 3-35: MEMCS Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
PD[29:14] (ED[15:0])	t_{ISED}	Data Input setup time	20			ns
	t_{IHED}	Data Input hold time	10.4			ns
PD30 (RDY)	t_{ISRDY}	RDY Input setup time	4			ns
	t_{IHRDY}	RDY Input hold time	2.4			ns

The reference clock of RDY is the internal clock.

3.5.5.2. Output Signal

Table. 3-36: MEMCS Output Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
PD[29:14] (ED[15:0])	t_{ODLYED}	Data Output delay time	-8		22.4	ns
PD[9:8] (XCS[1:0])	t_{ODLYCS}	Chip select Output delay time	-8		22.4	ns
PD[55:31] (EA[24:0])	t_{ODLYEA}	Address Output delay time	-8		22.4	ns
PD10 (XRD)	$t_{ODLYXRD}$	XRD Output delay time	-8		22.4	ns
PD[12:11] (XWR[1:0])	$t_{ODLYXWR}$	XWR[1:0] Output delay time	-8		22.4	ns
PD13 (XWE)	$t_{ODLYXWE}$	XWE Output delay time	-8		22.4	ns

The reference clock of output delay is the internal clock.

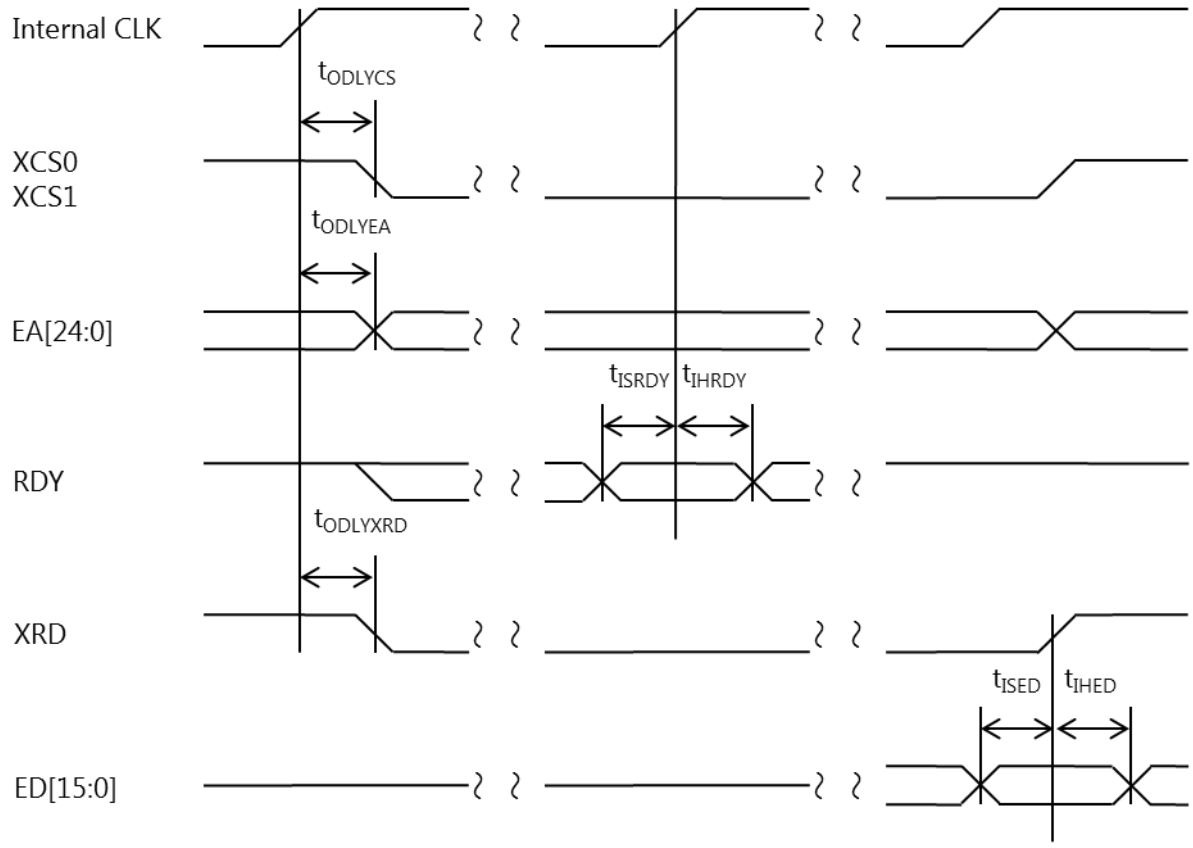


Figure. 3-30: MEMCS Signal Timing(Read)

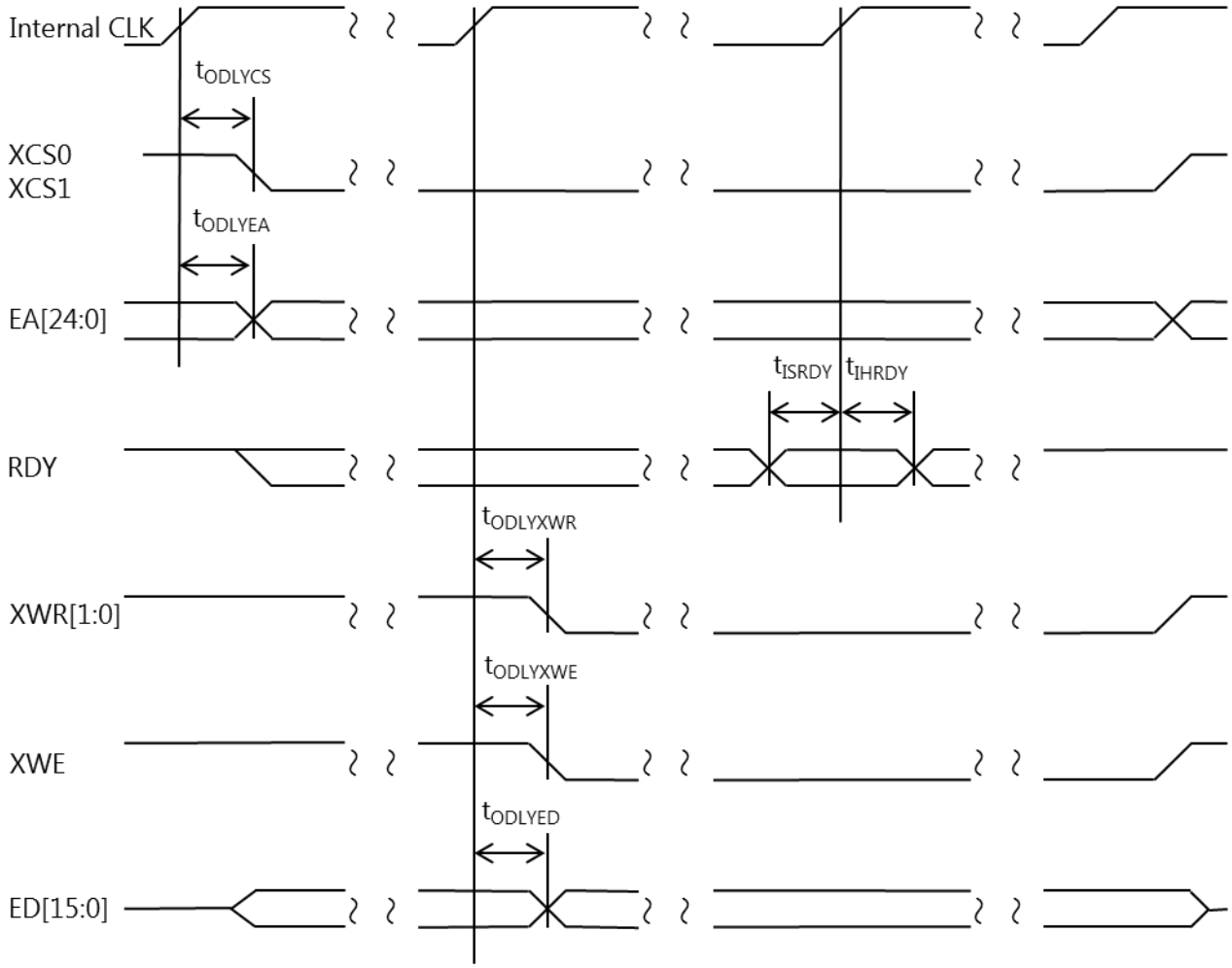


Figure. 3-31: MEMCS Signal Timing(Write)

3.5.6. FPDLink Signal Timing

3.5.6.1. Output Signal

Table. 3-37: FPDLink Output Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
FPD_DATP/N[3:0]	t_{ODS}	FPD_DATP/N output data skew	-0.15	—	0.15	ns

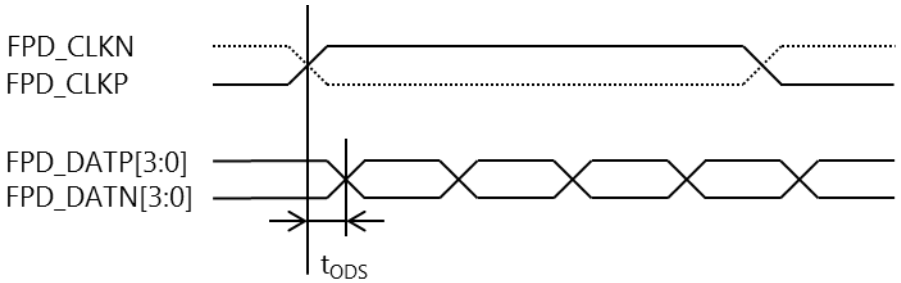


Figure. 3-32: FPDLink Signal Timing

3.5.7. GMAC Signal Timing

3.5.7.1. Clock

Table. 3-38: GMAC Clock

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
ET_RXCLK	t_{IWH}	ET_RXCLK H width (125MHz)	3.6			ns
	t_{IWL}	ET_RXCLK L width (125MHz)	3.6			ns
	t_{IWH}	ET_RXCLK H width (25MHz)	16			ns
	t_{IWL}	ET_RXCLK L width (25MHz)	16			ns
	t_{IWH}	ET_RXCLK H width (2.5MHz)	160			ns
	t_{IWL}	ET_RXCLK L width (2.5MHz)	160			ns
ET_GTXCLK	t_{OWH}	ET_GTXCLK H width (1000BASE)	3.6			ns
	t_{OWL}	ET_GTXCLK L width (1000BASE)	3.6			ns
	t_{OWH}	ET_GTXCLK H width (100BASE)	16			ns
	t_{OWL}	ET_GTXCLK L width (100BASE)	16			ns
	t_{OWH}	ET_GTXCLK H width (10BASE)	160			ns
	t_{OWL}	ET_GTXCLK L width (10BASE)	160			ns

3.5.7.2. Input Signal

Table. 3-39: GMAC Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
ET_RXD[3:0]	t_{ISRXD}	ET_RXD[3:0] Input setup time ET_RXCLK = 125MHz)	1.0			ns
	t_{IHRXD}	ET_RXD[3:0] Input hold time ET_RXCLK = 125MHz)	1.0			ns
	t_{ISRXD}	ET_RXD[3:0] Input setup time ET_RXCLK = 25MHz)	1.0			ns
	t_{IHRXD}	ET_RXD[3:0] Input hold time ET_RXCLK = 25MHz)	15.4			ns
	t_{ISRXD}	ET_RXD[3:0] Input setup time ET_RXCLK = 2.5MHz)	1.0			ns
	t_{IHRXD}	ET_RXD[3:0] Input hold time ET_RXCLK = 2.5MHz)	177.4			ns
ET_RXDV	t_{ISRXDV}	ET_RXDV Input setup time ET_RXCLK = 125MHz)	1.0			ns
	t_{IHRXDV}	ET_RXDV Input hold time ET_RXCLK = 125MHz)	1.0			ns
	t_{ISRXDV}	ET_RXDV Input setup time ET_RXCLK = 25MHz)	1.0			ns
	t_{IHRXDV}	ET_RXDV Input hold time ET_RXCLK = 25MHz)	15.4			ns
	t_{ISRXDV}	ET_RXDV Input setup time ET_RXCLK = 2.5MHz)	1			ns
	t_{IHRXDV}	ET_RXDV Input hold time ET_RXCLK = 2.5MHz)	177.4			ns

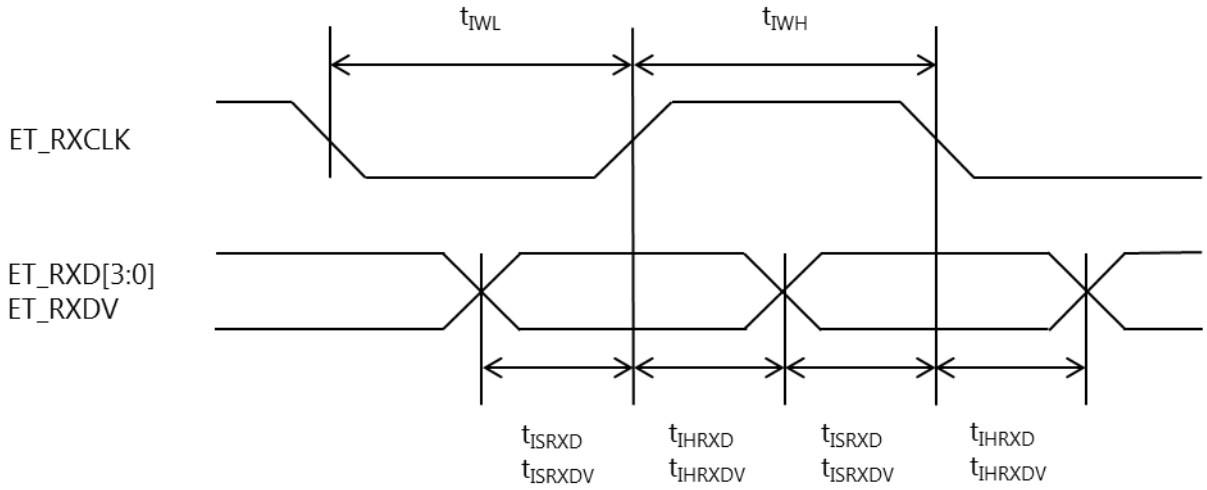


Figure. 3-33: GMAC Input Signal Timing

3.5.7.3. Output Signal

Table. 3-40: GMAC Output Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
ET_TXD[3:0]	$t_{ODLYTXD}$	ET_TXD[3:0] Output delay time	-0.5		0.5	ns
ET_TXEN	$t_{ODLYTXEN}$	ET_TXEN Output delay time	-0.5		0.5	ns

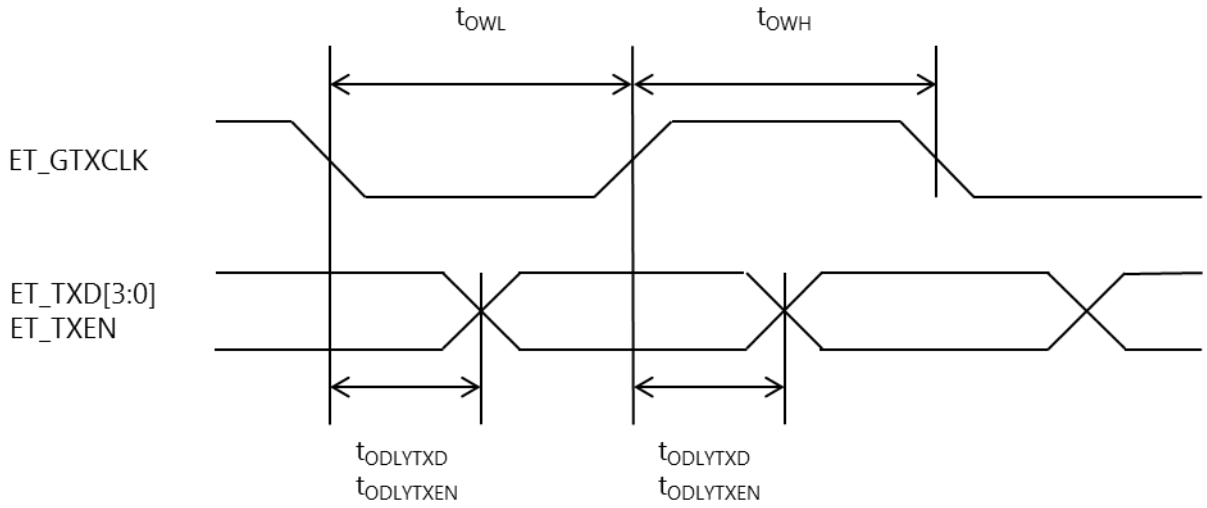


Figure. 3-34: GMAC Output Signal Timing

3.5.8. SDIO Signal Timing

3.5.8.1. Clock

Table. 3-41:SDIO Clock

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
SDIO_CLK	t_{OWH}	SDIO_CLK H width (SDR104)	1.5			ns
	t_{OWL}	SDIO _CLK L width (SDR104)	1.5			ns
	t_{OWH}	SDIO _CLK H width (SDR12/25/50)	6.0			ns
	t_{OWL}	SDIO _CLK L width (SDR12/25/50)	6.0			ns
	t_{OWH}	SDIO _CLK H width (DDR50)	9.0			ns
	t_{OWL}	SDIO _CLK L width (DDR50)	9.0			ns
	t_{OWH}	SDIO _CLK H width(High)	7.0			ns
	t_{OWL}	SDIO _CLK L width (High)	7.0			ns
	t_{OWH}	SDIO _CLK H width(Default)	10.0			ns
	t_{OWL}	SDIO _CLK L width (Default)	10.0			ns

3.5.8.2. Input Signal

Table. 3-42: SDIO Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
SDIO_DAT[3:0]	t_{ISDAT}	SDIO_DAT Input setup time (SDR12/25/50)	2.5			ns
		SDIO_DAT Input setup time (DDR50)	2.0			ns
	t_{IHDAT}	SDIO_DAT Input hold time SDR12/25/50,DDR50)	1.5			ns
SDIO_CMD	t_{ISCMD}	SDIO_CMD Input setup time (SDR12/25/50,DDR50)	2.5			ns
	t_{IHCMD}	SDIO_CMD Input hold time (SDR12/25/50,DDR50)	1.5			ns

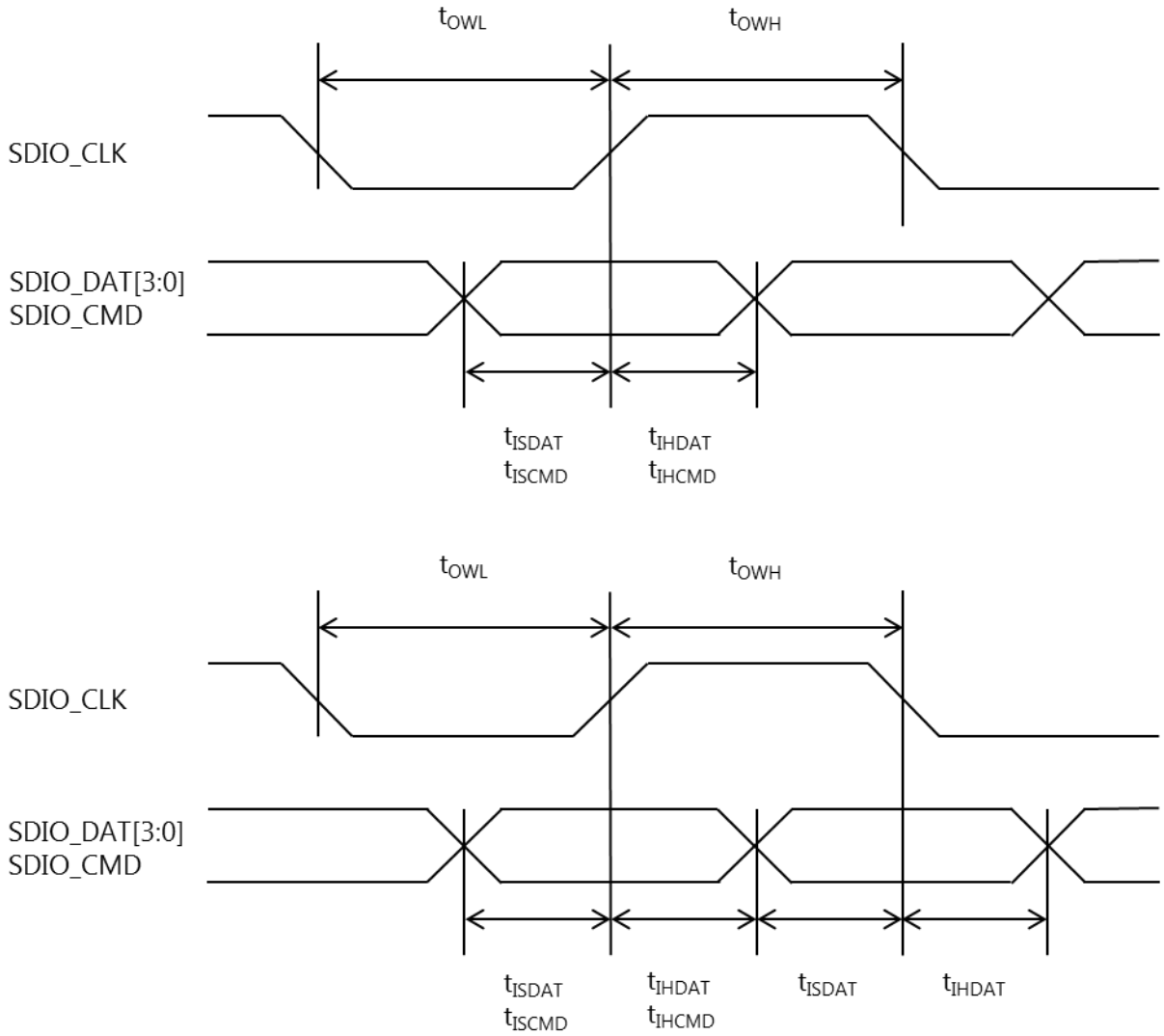


Figure. 3-35: SDIO Input Signal Timing

3.5.8.3. Output Signal

Table. 3-43: SDIO Output Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
SDIO_DAT[3:0] SDIO_CMD	$t_{ODLYDAT1}$ $t_{ODLYCMD1}$	SDIO_DAT/SDIO_CMD Output delay time (Default, High, SDR12/25) *1	1.05		3.75	ns
	$t_{ODLYDAT2}$ $t_{ODLYCMD2}$	SDIO _DAT/SDIO_CMD Output delay time (DDR50)*1	1.05		6.75	ns
	$t_{ODLYDAT3}$ $t_{ODLYCMD3}$	SDIO _DAT/SDIO_CMD Output delay time (SDR50,104)*2	1.05		3.35	ns

*1 : Division mode, Hold time care.
*2 : Non division mode, No HOLD time care.

These are the values for Buffer TYPE A, CL=10pF.

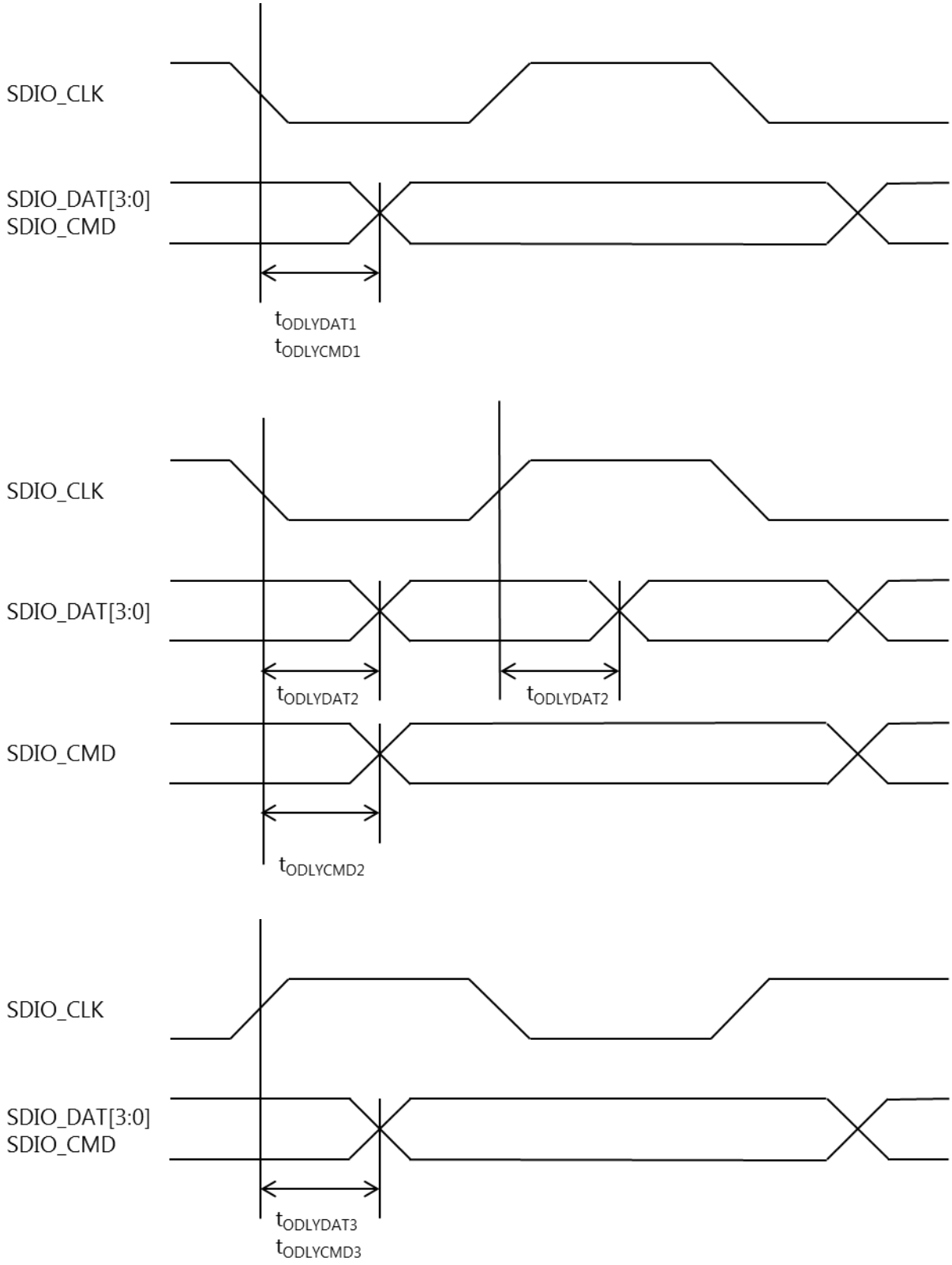


Figure. 3-36: SDIO Output Signal Timing

3.5.9. CSSYS Signal Timing

3.5.9.1. Clock

Table. 3-44: CSSYS Clock

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
PD60(TRACECLK)	t_{OWH}	TRACECLK H width	2.35			ns
	t_{OWL}	TRACECLK L width	2.35			ns

3.5.9.2. Output Signal

Table. 3-45: CSSYS Output Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
PD[59:44](TRACEDAT[15:0])	$t_{ODLYDAT}$	TRACEDAT Output delay time	0.75			ns
PD61(TRACECTL)	$t_{ODLYCTL}$	TRACECTL Output delay time	0.75			ns

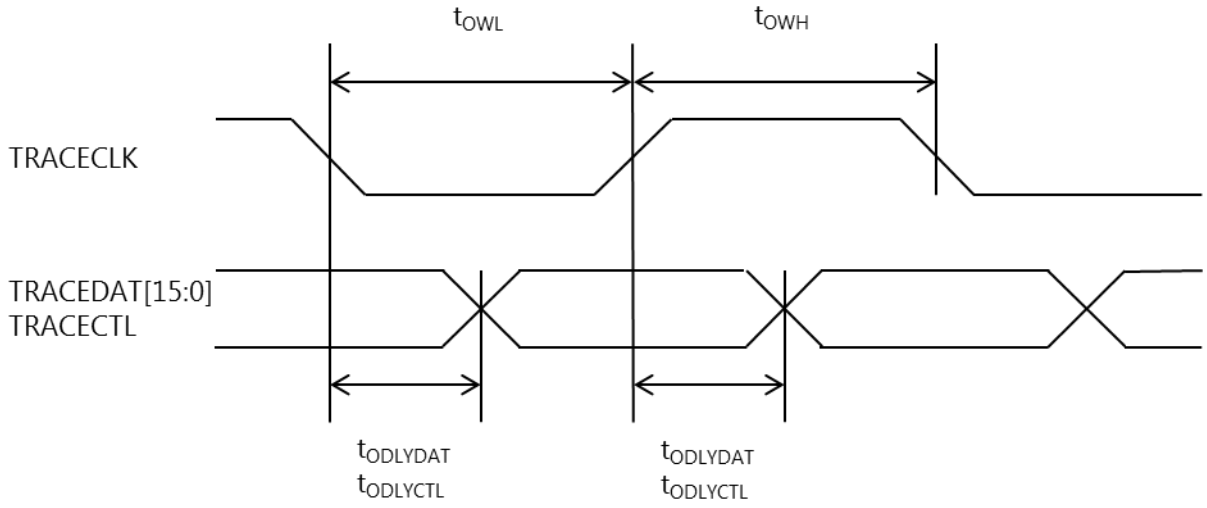


Figure. 3-37: CSSYS Signal Timing

3.5.10. SAIF(I2S) Signal Timing

3.5.10.1. Clock

Table. 3-46: I2S Clock

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
I2S_SCLK	$t_{ICYCSCLK}$	I2S_SCLK cycle (Slave)	40.69			ns
	$t_{IWHSCLK}$	I2S_SCLK H width (Slave) *1	0.45*T		0.55*T	ns
	$t_{IWLSCLK}$	I2S_SCLK L width (Slave) *1	0.45*T		0.55*T	ns
	$t_{OCYCSCLK}$	I2S_SCLK cycle (Master) *2	20			ns
	$t_{OWHSCLK}$	I2S_SCLK H width (Master) *1	0.45*T		0.55*T	ns
	$t_{OWLSCLK}$	I2S_SCLK L width (Master) *1	0.45*T		0.55*T	ns

*1 T: The I2S_SCLK cycle is indicated

*2 In the internal clock mode, since HCLK is 200MHz, 1/4 frequency division ratio 50MHz is the usable upper limit. (ECKM=0x0, CKRT=0x02)

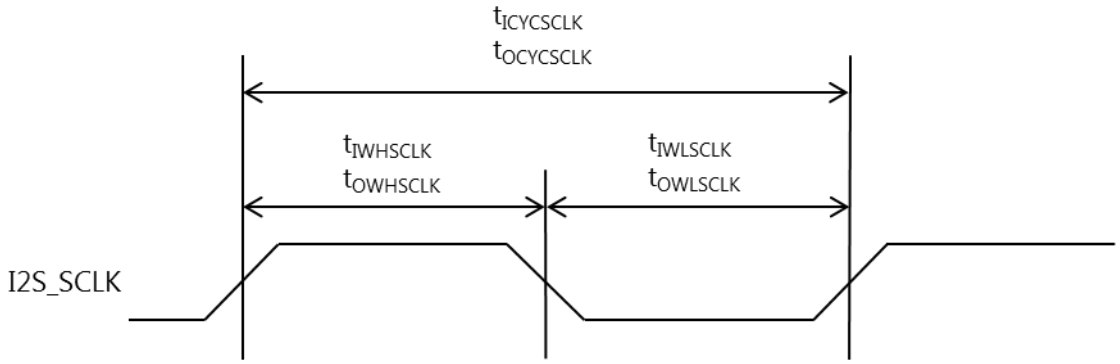


Figure. 3-38: I2S Clock Timing

3.5.10.2. Input Signal

Table. 3-47: I2S Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
I2S0_FSYN I2S1_FSYN	$t_{ISFSYNS}$	I2S0/1_FSYN Input setup time (Slave)	6			ns
	$t_{IHFSYNS}$	I2S0/1_FSYN Input hold time (Slave)	0			ns
I2S0_SDO I2S1_SDO	t_{ISSDO}	I2S0/1_SDO Input setup time (Slave) (Master)	6			ns
	t_{IHSDO}	I2S0/1_SDO Input hold time (Slave) (Master)	0			ns

3.5.10.3. Output Signal

Table. 3-48: I2S Output Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
I2S0_FSYN I2S1_FSYN	$t_{ODLYFSYNM}$	I2S0/1_FSYN Output delay time (Master)	0		14	ns
I2S0_SDO I2S1_SDO	$t_{ODLYSDOS0}$	I2S0/1_SDO Output delay time. except the first bit of a transmit frame. (Slave)	0		14	ns
	$t_{ODLYSDOS1}$	I2S0/1_SDO Output delay time. the first bit of a transmit frame when FSPH bit of CNTREG register is 0. (Slave)	0		14	ns
	$t_{ODLYSDOS2}$	I2S0/1_SDO Output delay time. the first bit of a transmit frame when FSPH bit of CNTREG register is 1. (Slave)	0		14	ns
	$t_{ODLYSDOM0}$	I2S0/1_SDO Output delay time. except the first bit of a transmit frame. (Master)	0		14	ns
	$t_{ODLYSDOM1}$	I2S0/1_SDO Output delay time. the first bit of a transmit frame when FSPH bit of CNTREG register is 0. (Master)	0		14	ns
	$t_{ODLYSDOM2}$	I2S0/1_SDO Output delay time. the first bit of a transmit frame when FSPH bit of CNTREG register is 1. (Master)	0		14	ns

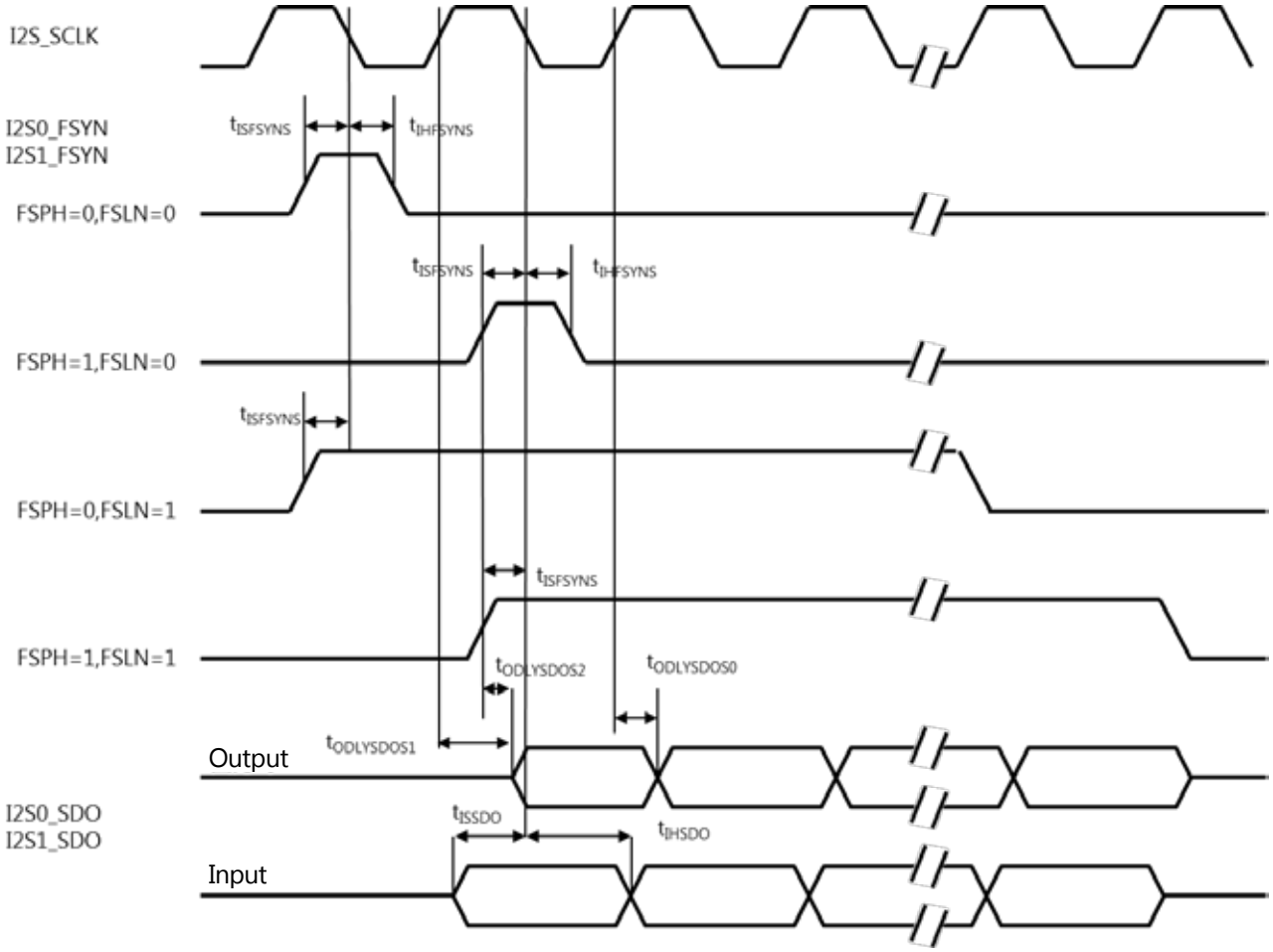


Figure. 3-39: I2S Signal Timing (Slave)

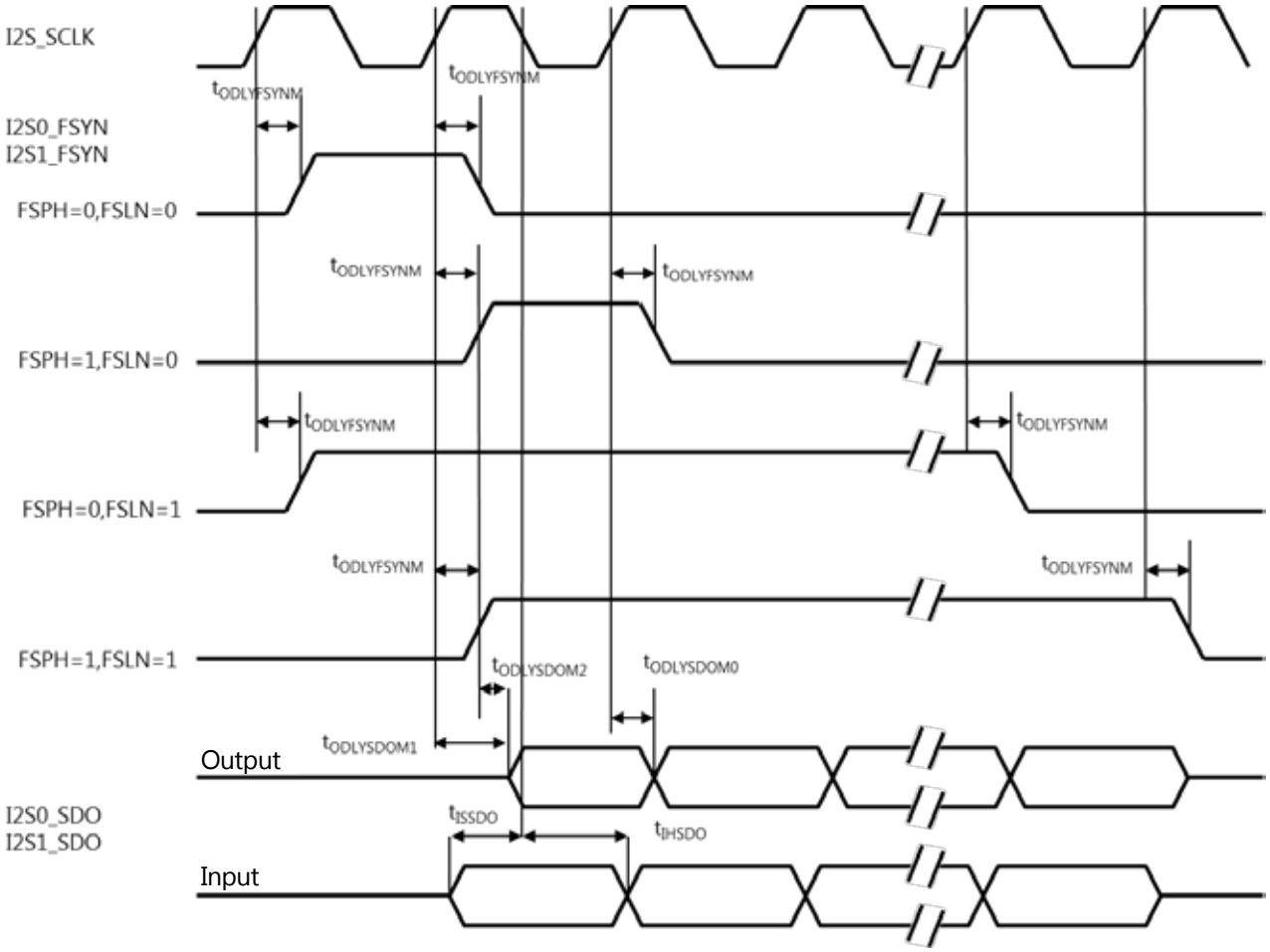


Figure. 3-40: I2S Signal Timing(Master)

3.5.11. UART Signal Timing

3.5.11.1. Input Signal

Table. 3-49: UART Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
SIN0 PD17(RXD1) PD25(RXD2) XCTS0 PD22(CTS1) PD30(CTS2) PD8(DCD0) PD16(DCD1) PD24(DCD2) PD12(DSR0) PD20(DSR1) PD28(DSR2) PD15(RI0) PD23(RI1) PD31(RI2)	t_{ISSIN0} t_{ISRXD1} t_{ISRXD2} t_{ISCTS0} t_{ISCTS1} t_{ISCTS2} t_{ISDCD0} t_{ISDCD1} t_{ISDCD2} t_{ISDSR0} t_{ISDSR1} t_{ISDSR2} t_{ISRI0} t_{ISRI1} t_{ISRI2}	Data Input setup time	26			ns
	t_{IHSIN0} t_{IHRXD1} t_{IHRXD2} t_{IHCTS0} t_{IHCTS1} t_{IHCTS2} t_{IHDCD0} t_{IHDCD1} t_{IHDCD2} t_{IHDSR0} t_{IHDSR1} t_{IHDSR2} t_{IHRI0} t_{IHRI1} t_{IHRI2}	Data Input hold time	4			ns

The reference clock is the internal clock.

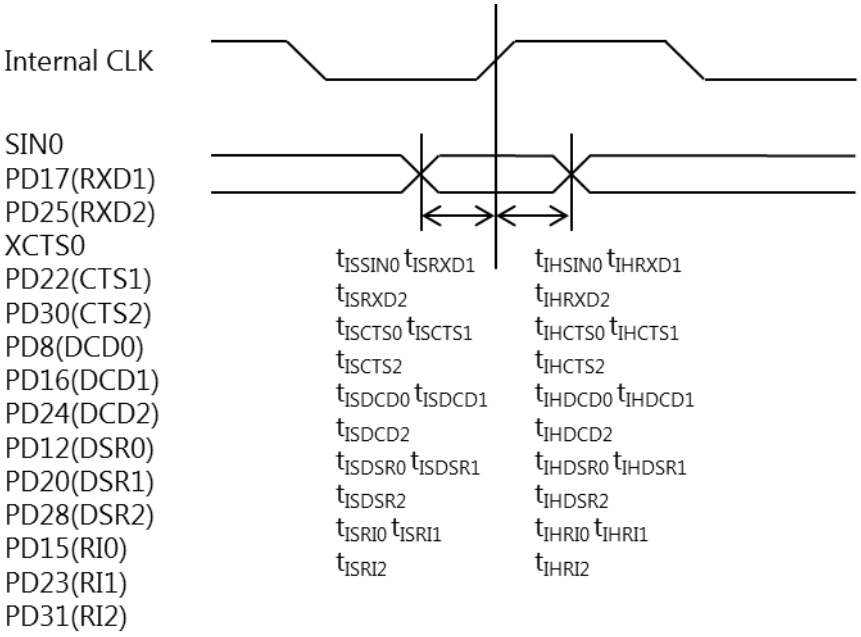


Figure. 3-41: UART Input Signal Timing

3.5.11.2. Output Signal

Table. 3-50: UART Output Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
SOUT0 PD18(TXD1) PD26(TXD2) PD11(DTR0) PD19(DTR1) PD27(DTR2) XRTS0 PD21(RTS1) PD29(RTS2)	$t_{ODLYSOUT0}$ $t_{ODLYTXD1}$ $t_{ODLYTXD2}$ $t_{ODLYDTR0}$ $t_{ODLYDTR1}$ $t_{ODLYDTR2}$ $t_{ODLYRTS0}$ $t_{ODLYRTS1}$ $t_{ODLYRTS2}$	Data Output delay time	0		30	ns

The reference clock of output delay is the internal clock.

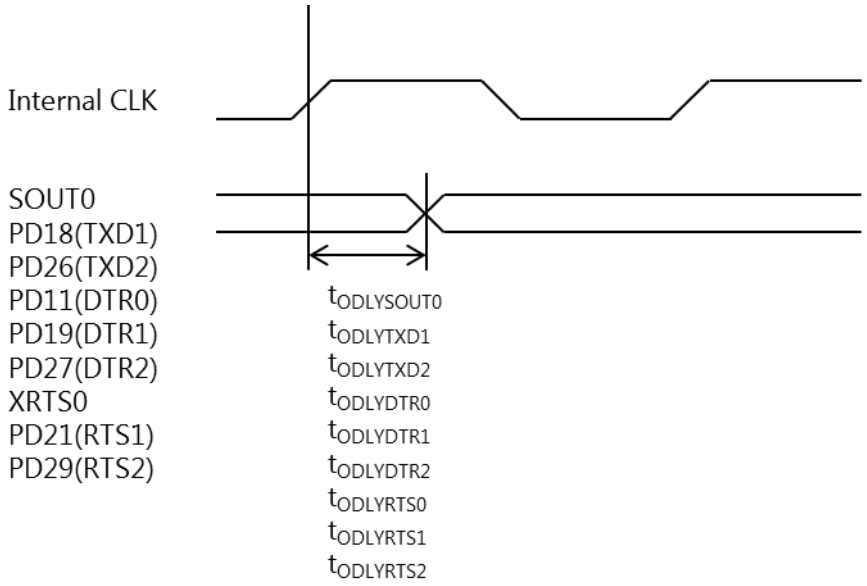


Figure. 3-42: UART Output Signal Timing

3.5.12. DDR3L Signal Timing

The descriptions in this document have been given taking the value of specific byte as the reference data. For the PHY set values and the values of different bytes, see "MB86S72 AC spec calculation guide" and "MB86S72 Timing Design Kit".

3.5.12.1. Clock

Table. 3-51: DDR3L Clock

Signal	Symbol	Value	Unit
DDR_CLKO[3:0] XDDR_CLKO[3:0]	t_{CK}	1500	ps

3.5.12.2. Control, Command, Address parameters

Table. 3-52: DDR3L Control, Command, Address parameters

Signal	Symbol	Value	Unit
DDR_CKE[3:0] XDDR_CS[3:0] DDR_ODT[3:0] XDDR_WE XDDR_CAS XDDR_RAS XDDR_RESET	tphy_ACCSkew_CTRL(+)	251	ps
	tphy_ACCSkew_CTRL(-)	-126	ps
	tphy_IS_CTRL	499	ps
	tphy_IH_CTRL	624	ps
DDR_ADD[15:0] DDR_BA[2:0]	tphy_ACCSkew_CA(+)	280	ps
	tphy_ACCSkew_CA(-)	-115	ps
	tphy_IS_CA(1T timing)	470	ps
	tphy_IH_CA(1T timing)	635	ps
	tphy_IS_CA(2T timing)	1970	ps
	tphy_IH_CA(2T timing)	635	ps

3.5.12.3. Data eye parameters

Table. 3-53: Data eye parameters

Signal	Symbol	Value	Unit
DDR_DQ[63:0] DDR_DQM[7:0]	tphy_DQSDQQ(+)	67	ps
	tphy_DQSDQQ(-)	-67	ps
	tphy_WDS	308	ps
	tphy_WDH	308	ps
	tphy_RDS	337	ps
	tphy_RDH	413	ps

3.5.12.4. Domain cross timing parameters

Table. 3-54: Domain cross timing parameters

Signal	Symbol	Value	Unit
DDR_DQ[63:0]	tphy_CKDQS(min)	-293	ps
	tphy_CKDQS(max)	293	ps
	tphy_RTT_Gate(min)	1453	ps
	tphy_RTT_Gate(max)	3247	ps

CK-CTRL

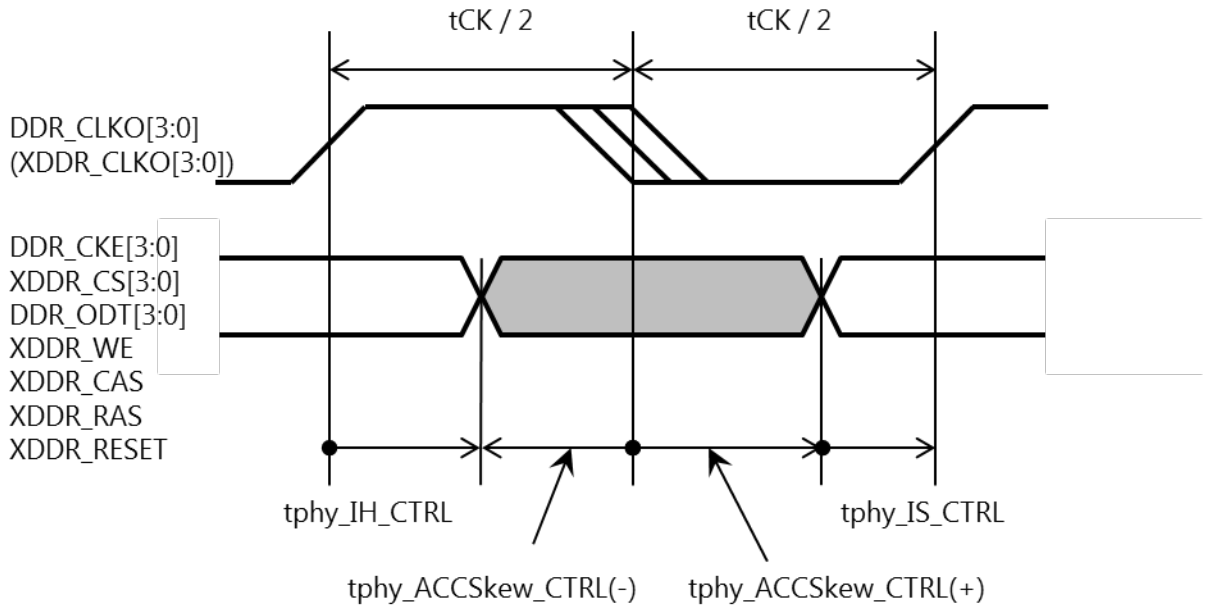


Figure. 3-43: CK-CTRL Timing

CK-CA (2T timing)

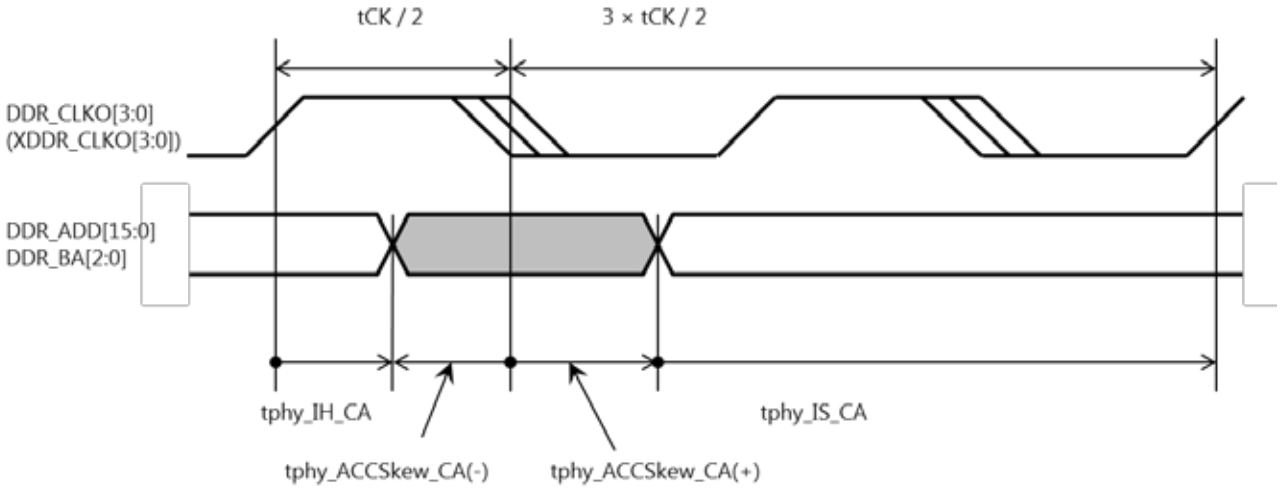


Figure. 3-44: CK-CA (2T timing)

TXDQS-TXDQ,TXDM

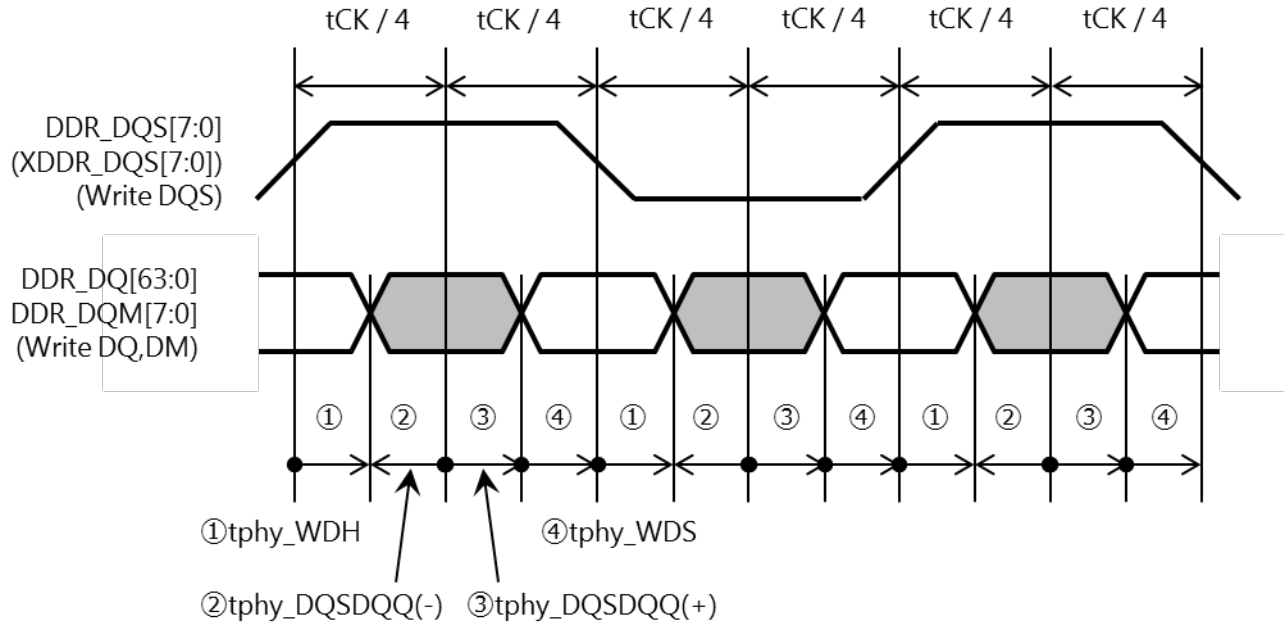


Figure. 3-45: TXDQS-TXDQ,TXDM

RXDQS-RXDQ

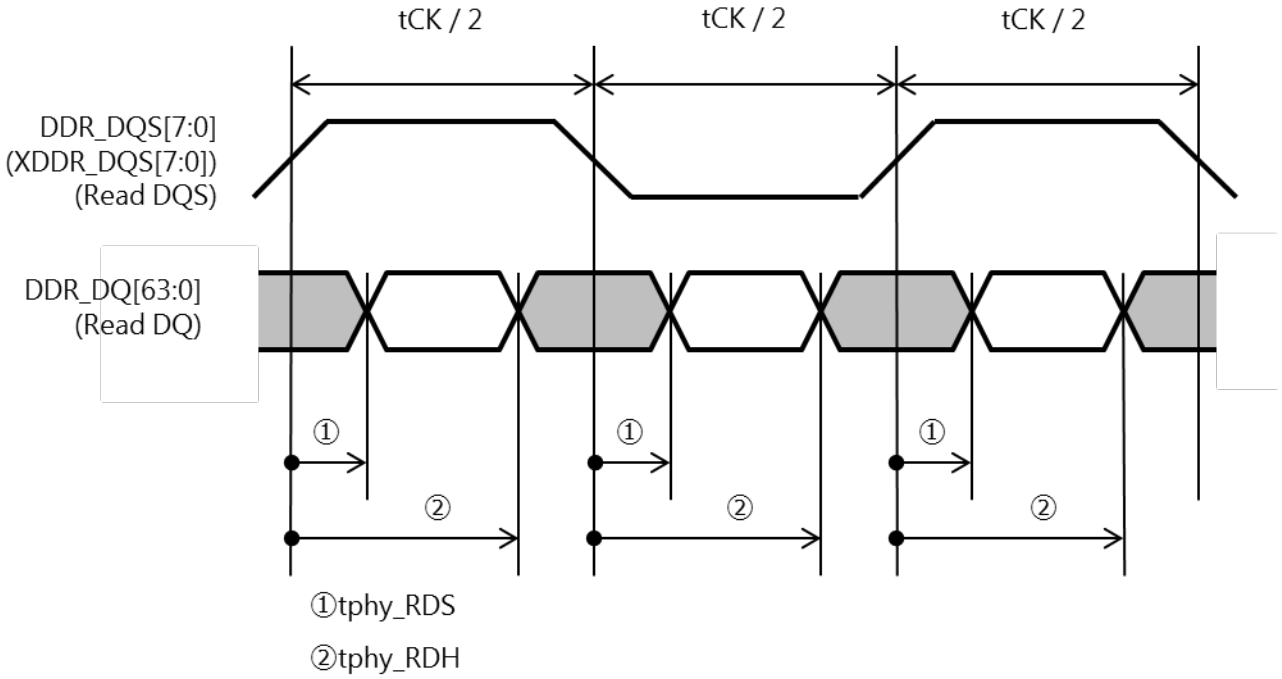


Figure. 3-46: RXDQS-RXDQ

CK-TXDQS (Write Leveling is enabled)

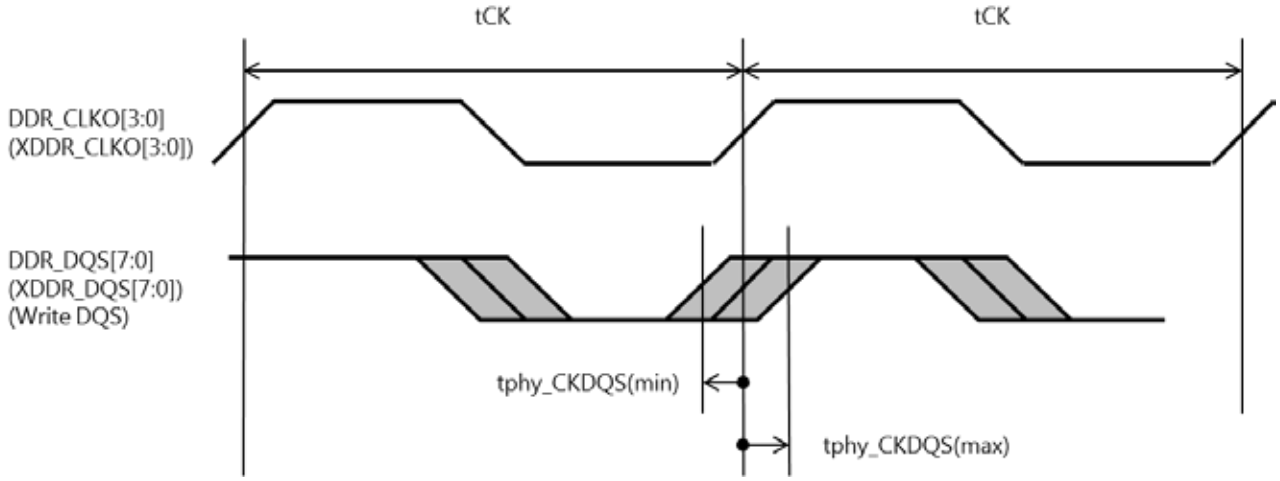


Figure. 3-47: CK-TXDQS (Write Leveling is enabled)

Gate timing

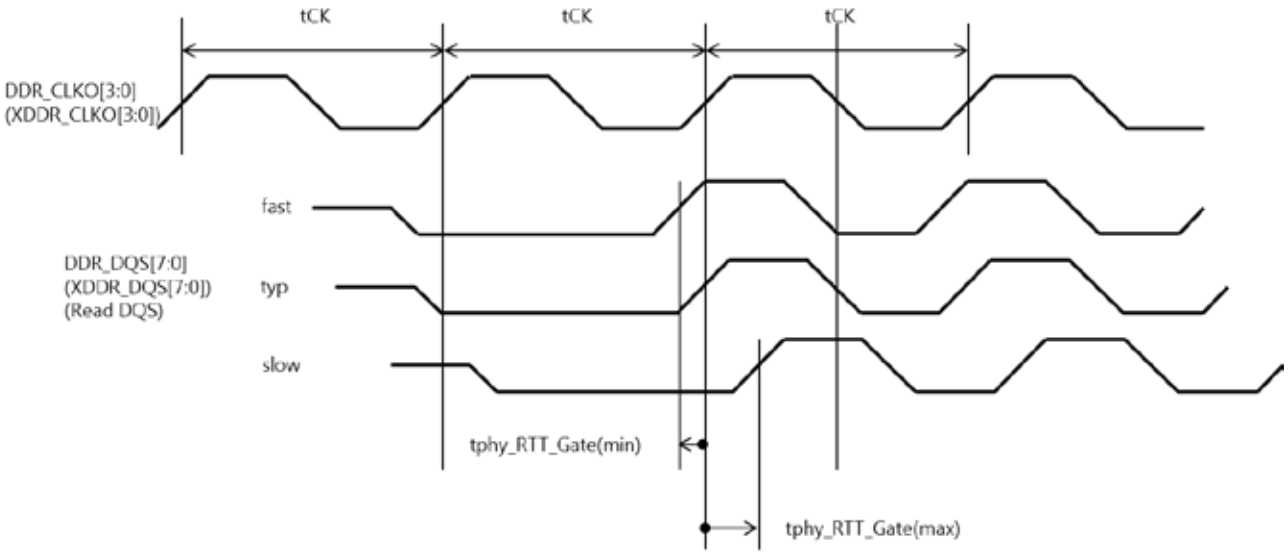


Figure. 3-48: Gate timing

3.5.13. I2C Signal Timing

3.5.13.1. Bus Signal

Table. 3-55: I2C Bus Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
I2C0_SDA I2C1_SDA I2C2_SDA	t_{S2SDAI}	SDAI setup time (Standard Mode)	250 (*1)			ns
		SDAI setup time (Fast Mode)	100 (*1)			ns
	t_{H2SDAI}	SDAI hold time (Standard Mode)	0.0 (*1)			ns
		SDAI hold time (Fast Mode)	0.0 (*1)			ns
	t_{WBFI}	Bus free time (Standard Mode)	4.7 (*1)			us
		Bus free time (Fast Mode)	1.3 (*1)			us
	t_{H2SDAO}	SDAO hold time	5			PLCK (*4)
I2C0_SCL I2C1_SCL I2C2_SCL	t_{CSCLI}	SCLI cycle time (Standard Mode)	10 (*1)			us
		SCLI cycle time (Fast Mode)	2.5 (*1)			us
	t_{WHSCLI}	SCLI H width (Standard Mode)	4.0 (*1)			us
		SCLI H width (Fast Mode)	0.6 (*1)			us
	t_{WLSCLI}	SCLI L width (Standard Mode)	4.7 (*1)			us
		SCLI L width (Fast Mode)	1.3 (*1)			us
	t_{CSCLO}	SCLO cycle time (Standard Mode)	2*m+2 (*2)			PLCK (*4)
		SCLO cycle time (Fast Mode)	int(1.5*m)+2 (*2)			PLCK (*4)
	t_{WHSCLO}	SCLO H width (Standard Mode)	m+2 (*2)			PLCK (*4)
		SCLO H width (Fast Mode)	int(0.5*m)+2 (*2)			PLCK (*4)
	t_{WLSCLO}	SCLO H width (Fast Mode)	m (*2)			PLCK (*4)
		SCLO L width (Standard Mode)	m (*2)			PLCK (*4)

I2C0_SCL I2C1_SCL I2C2_SCL	t_{S2SCLI}	SCLI setup time (Standard Mode)	4.7 (*1)			us
		SCLI setup time (Fast Mode)	0.6 (*1)			us
	t_{H2SCLI}	SCLI hold time (Standard Mode)	4.0 (*1)			us
		SCLI hold time (Fast Mode)	0.6 (*1)			us
	t_{S2SCLO}	SCLO setup time (Standard Mode)	m+2 (*2)			PLCK (*4)
		SCLO setup time (Fast Mode)	int(0.5*m)+2 (*2)			PLCK (*4)
	t_{H2SCLO}	SCLO hold time (Standard Mode)	m-3 (*2)			PLCK (*4)
			CS-(2*FS+1) (*3)			PLCK (*4)
		SCLO hold time (Fast Mode)	int(0.5*m)-3 (*2)			PLCK (*4)
			int(0.5*CS) -(2*FS+1) (*3)			PLCK (*4)

(*1) I^{2}C bus specifications value.
(*2) See the clock control register (CCR) for the value of m.
(*3) When the extended CS register (CSR) and the system clock frequency register (FSR) are used.
(*4) PCLK=APB bus clock cycle.

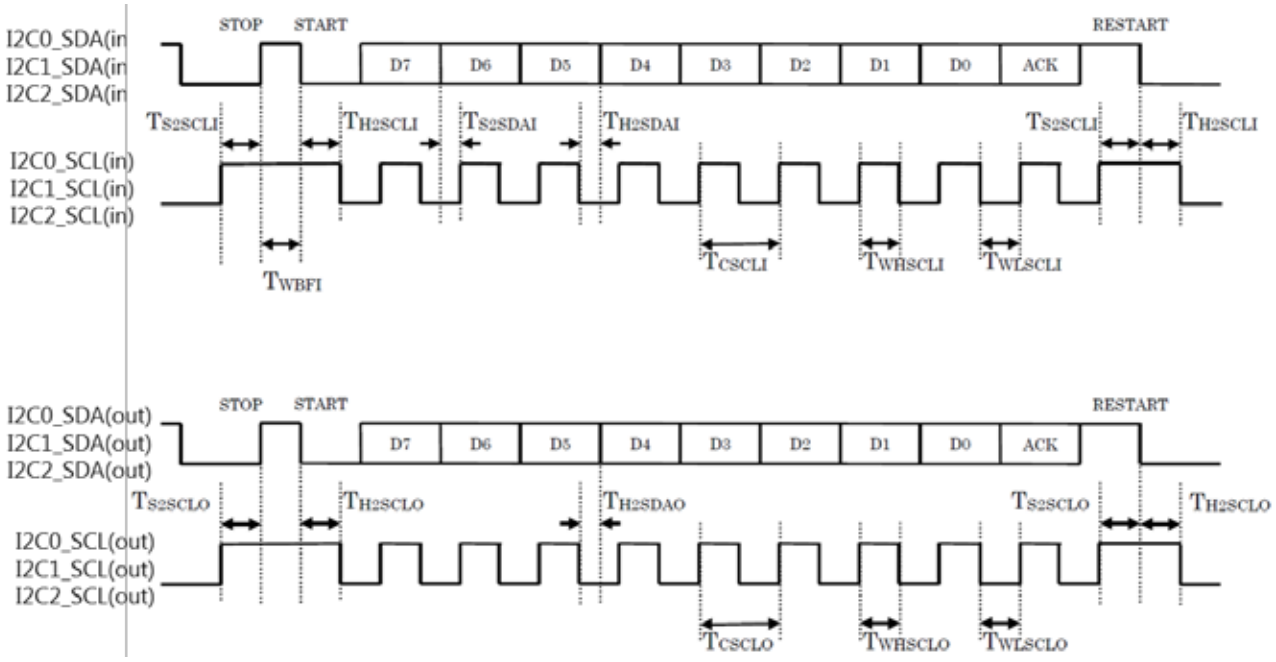


Figure. 3-49: I2C Bus Signal Timing

Table 3-56: I2C Bus Signal High Speed supported version

Signal	Symbol	Description	Value		Unit
			Min.	Max.	
I2C3_SDA I2C4_SDA	$T_{SU:DAT}$	SDAI(SCLI) DATA(ADDRESS) setup time (Standard Mode)	250	—	ns
		SDAI(SCLI) DATA(ADDRESS) setup time (Fast Mode)	100	—	ns
		SDAI(SCLI) DATA(ADDRESS) setup time (High Speed Mode)	10	—	ns
	$T_{HD:DAT}$	SDAI(SCLI) DATA(ADDRESS) hold time (Standard Mode)	0	3450	ns
		SDAI(SCLI) DATA(ADDRESS) hold time (Fast Mode)	0	900	ns
		SDAI(SCLI) DATA(ADDRESS) hold time (High Speed Mode)	0	70	ns
I2C3_SCL I2C4_SCL	f_{scl}	SCLI Frequency (Standard Mode)		100	kHz
		SCLI Frequency (Fast Mode)		400	kHz
		SCLI Frequency (High Speed Mode)		2	MHz
	T_{HIGH}	SCLI H width (Standard Mode)	4000	—	ns
		SCLI H width (Fast Mode)	600	—	ns
		SCLI H width (High Speed Mode)	60	—	ns
	T_{LOW}	SCLI L width (Standard Mode)	4700	—	ns
		SCLI L width (Fast Mode)	1300	—	ns
		SCLI L width (High Speed Mode)	160	—	ns
	$T_{SU:STA}$	SCLI(SDAI) repeated START condition setup time (Standard Mode)	4700	—	ns
		SCLI(SDAI) repeated START condition setup time (Fast Mode)	600	—	ns
		SCLI(SDAI) repeated START condition setup time (High Speed Mode)	160	—	ns
	$T_{HD:STA}$	SCLI(SDAI) repeated START condition hold time (Standard Mode)	4000	—	ns
		SCLI(SDAI) repeated START condition hold time (Fast Mode)	600	—	ns
		SCLI(SDAI) repeated START condition hold time (High Speed Mode)	160	—	ns

	T_{BUF}	SCLI(SDAI) bus free time (Standard Mode)	4700	—	ns
		SCLI(SDAI) bus free time (Fast Mode)	1300	—	ns
		SCLI(SDAI) bus free time (High Speed Mode)	—	—	ns
	$T_{SU:STO}$	SCLI(SDAI) STOP condition setup time (Standard Mode)	4000	—	ns
		SCLI(SDAI) STOP condition setup time (Fast Mode)	600	—	ns
		SCLI(SDAI) STOP condition setup time (High Speed Mode)	160	—	ns

The values above are those of I^2C bus specifications.

Table 3-57: I2C Bus Signal High Speed supported version

Signal	Symbol	Description	Setting value	Unit
I2C3_SDA I2C4_SDA I2C3_SCL I2C4_SCL	TO_{fscl}	SCLO DATA(ADDRESS) clock cycle time Standard Mode Fast Mode High Speed Mode	$TO_{LOW} + TO_{HIGH}$	PCLK
	TO_{HIGH}	SCLO DATA(ADDRESS) clock H width Standard Mode Fast Mode	THW[15:0] + NF[4:0] + 6	PCLK
		High Speed Mode	THWH[7:0] + NFH[2:0] + 6	
	TO_{LOW}	SCLO DATA(ADDRESS) clock L width Standard Mode Fast Mode	TLW[15:0] + 2	PCLK
		High Speed Mode	TLWH[7:0] + 2	
	$TO_{SU:STA}$	SCLO(SDAO) repeated START condition setup time Standard Mode Fast Mode	NF[4:0] + TRS[15:0] +6	PCLK
		High Speed Mode	NFH[2:0] + TRSH[7:0] +6	
		Master Code + immediately after NAK	NF[4:0] + TRSH[7:0] +6	
	$TO_{HD:STA}$	SCLO(SDAO) repeated START condition hold time Standard Mode Fast Mode	TSH[15:0] + 3	PCLK
		High Speed Mode	TSHH[7:0] + 3	
	$TO_{HD:DAT}$	SDAO DATA(ADDRESS) hold time Standard Mode Fast Mode	NF[4:0] + 5	PCLK
		High Speed Mode	2	
	TO_{DATA1}	DATA transfer time1	4	PCLK

	Standard Mode		
	Fast Mode		
	High Speed Mode		
$TO_{SU:DAT1}$	SDAO DATA(ADDRESS) setup time nor		
	Standard Mode	TLW[15:0] – NF[4:0] -3	PCLK
	Fast Mode		
	High Speed Mode	TLWH[7:0]	
$TO_{SU:DAT2}$	SDAO DATA(ADDRESS) setup time After interrupt cancellation		
	Standard Mode	TLW[15:2] + 1	PCLK
	Fast Mode		
	High Speed Mode	TLWH[7:2] + 1	
TO_{STOP1}	STOP condition time 1		
	Standard Mode	4	PCLK
	Fast Mode		
	High Speed Mode		
TO_{STOP2}	STOP condition time 2		
	Standard Mode	TLW[15:2] + 1	PCLK
	Fast Mode		
	High Speed Mode	TLWH[7:2] + 1	
$TO_{SU:STO}$	STOP condition setup time		
	Standard Mode	NF[4:0] + TPS[15:0] + 6	PCLK
	Fast Mode		
	High Speed Mode	NFH[2:0] + TPSH[7:0] + 6	
TO_{BUF}	START condition setup time bus free time		
	Standard Mode	TBF[15:0] + 7	PCLK
	Fast Mode		
$TO_{RESTART1}$	repeated START condition setup time 1		
	Standard Mode	TLW[15:2] + 5	PCLK
	Fast Mode		
	High Speed Mode	TLWH[7:2] + 5	

Each AC specification setting register should be set to meet I^2C bus standard.

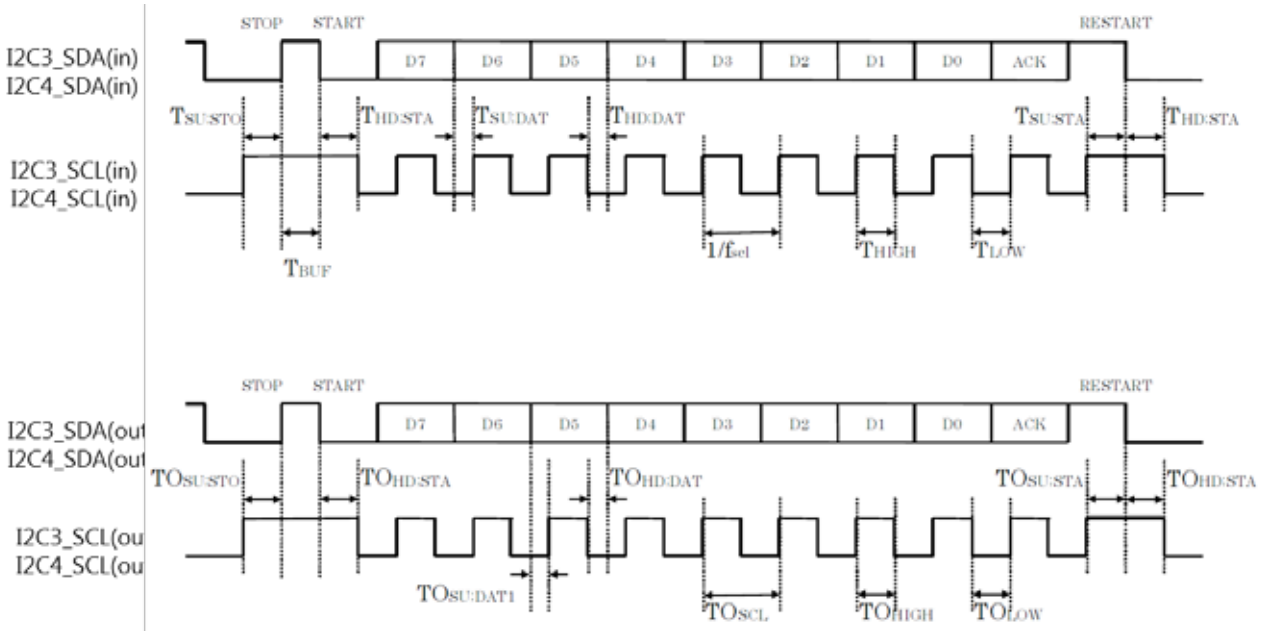
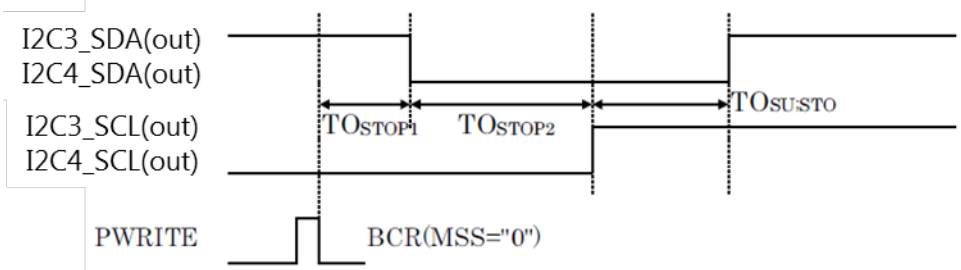
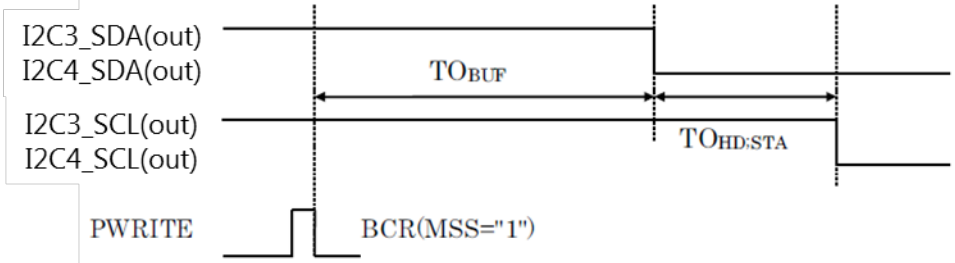


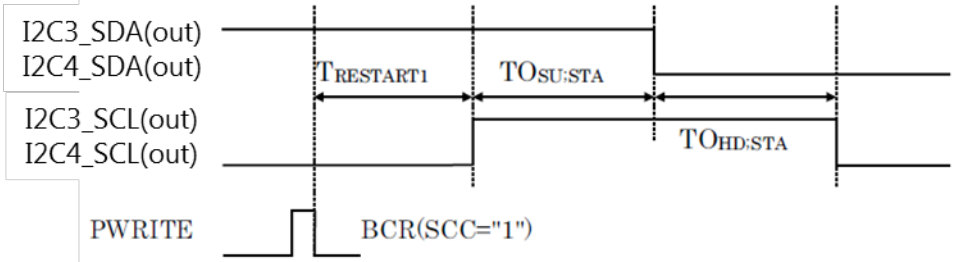
Figure 3-50: I2C Bus Signal Timing High Speed supported version



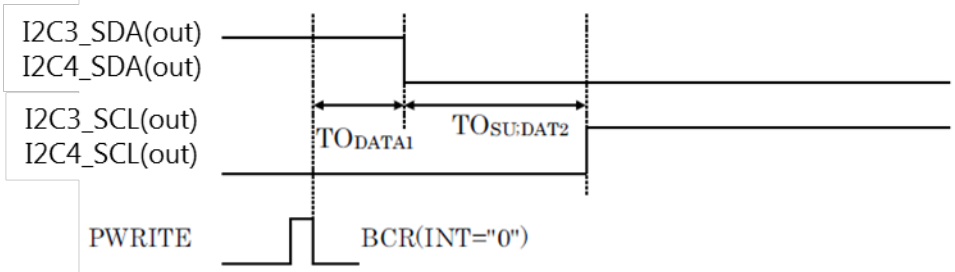
Timing to generate a stop condition



Timing to generate a start condition



Timing to generate an iterative start condition



Timing to send data after an interrupt

Figure 3-51: I2C Bus Signal Timing High Speed supported version

4. Power Supply Sequence

Power supply sequence is the order for multiple power supplies to be turned on/off when they are used in one LSI. If the order for power supplies to be turned on/off is not observed, penetrating through current will be generated in circuits or illegal output will be generated, causing a problem in reliability of behavior or products.

4.1. Order of Turning ON/OFF VDDE-VDDI Power Supplies

4.1.1. PLL

The power supplies should be turned on/off in the following order.

Powering on: VDD_SCB→AVD_PLL1/AVD_PLL2
VDD→AVD_PLL3/AVD_PLL5/AVD_PLL7/AVD_PLL8
VDD_FPD→AVD_PLL4

Powering off: AVD_PLL1/AVD_PLL2→VDD_SCB,
AVD_PLL5/AVD_PLL7/AVD_PLL8→VDD
AVD_PLL4→VDD_FPD

If the above order of turning on/off power supplies cannot be observed, the interval between turning on and turning off should be 10ms or below.

Caution) After powering on, perform reset to initialize circuits.

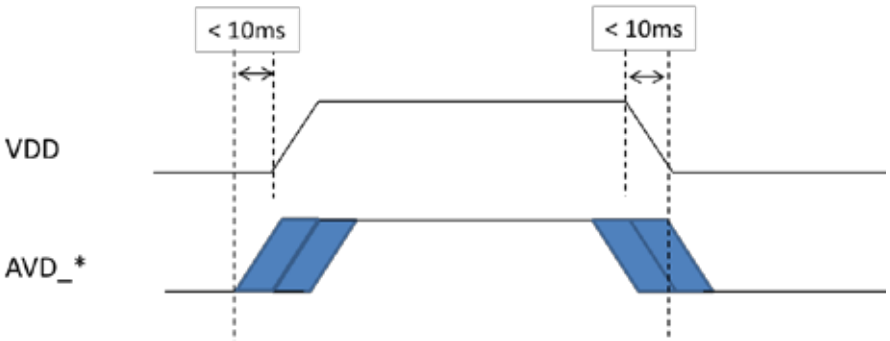


Figure 4-1: Order of turning ON/OFF power supplies for PLL

4.1.2. Temperature Sensor

The power supplies should be turned on/off in the following order.
Powering on: VDD_SCB→AVDH_*
Powering off: AVDH_*→VDD_SCB
If the above order of turning on/off power supplies cannot be observed, the interval between turning on and turning off should be 100us or below.

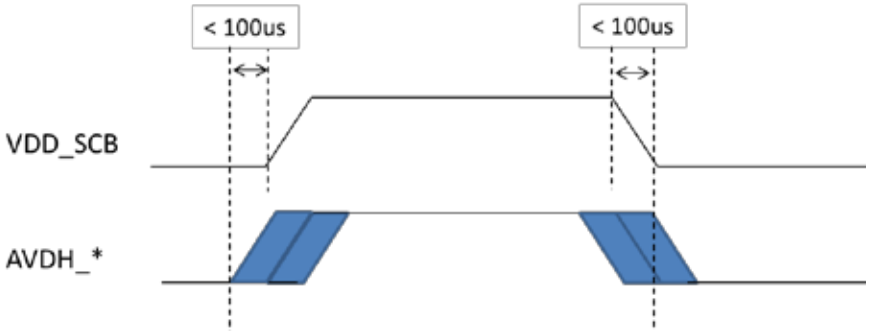


Figure 4-2: Order of turning ON/OFF power supplies for Temperature Sensors

4.1.3. SDIO0

The power supplies should be turned on/off in the following order.
Powering on: VDD→VDE_SDIO0
Powering off: VDE_SDIO0→VDD
If the above order of turning on/off power supplies cannot be observed, the interval between turning on and turning off should be 100ms or below.
Caution) Do not ever perform the selection of MSEL in VDE_SDIO0=3.3V state.

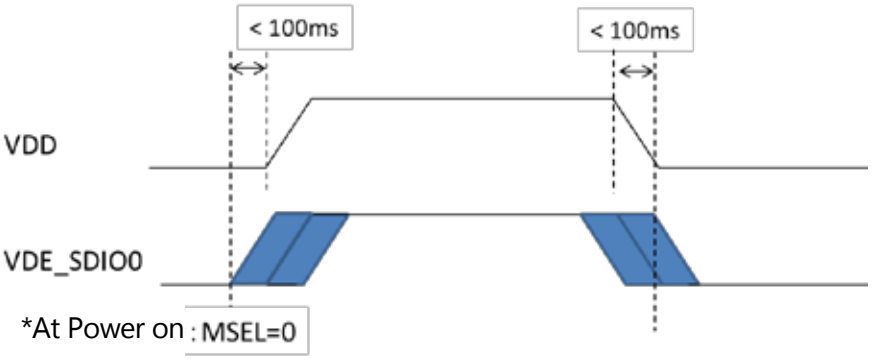


Figure 4-3: Order of turning ON/OFF power supplies for SDIO0

The speed of powering on (the time for getting to full amplitude) should be 50us or above.

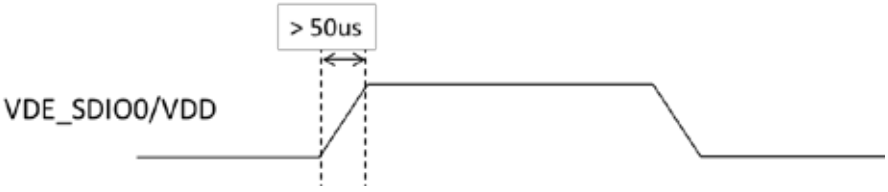


Figure 4-4: Speed of turning ON power supplies for SDIO0

4.1.4. SDIO1

The power supplies should be turned on/off in the following order.
Powering on: VDD_SCB→VDE_SDIO1
Powering off: VDE_SDIO1→VDD_SCB
If the above order of turning on/off power supplies cannot be observed, the interval between turning on and turning off should be 100ms or below.
Caution) Do not ever perform the selection of MSEL in VDE_SDIO1=3.3V state.

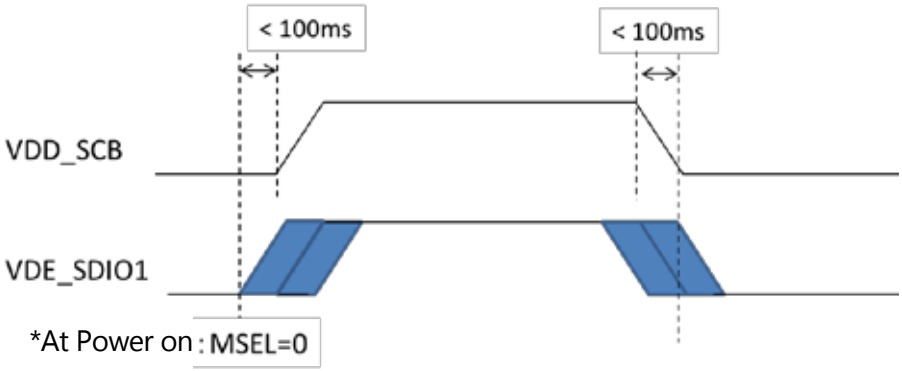


Figure 4-5: Order of turning ON/OFF power supplies for SDIO1

The speed of powering on (the time for getting to full amplitude) should be 50us or above.

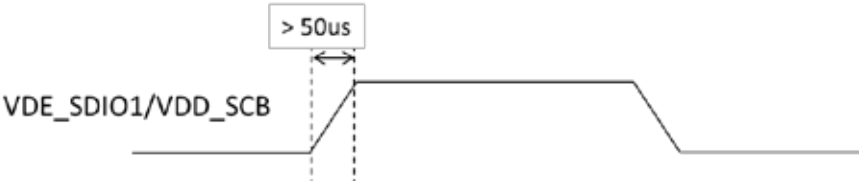


Figure 4-6: Speed of turning ON power supplies for SDIO1

4.1.5. EMMC

The power supplies should be turned on/off in the following order.

Powering on: VDD_SCB→VDE

Powering off: VDE→VDD_SCB

If the above order of turning on/off power supplies cannot be observed, the interval between turning on and turning off should be 100ms or below.

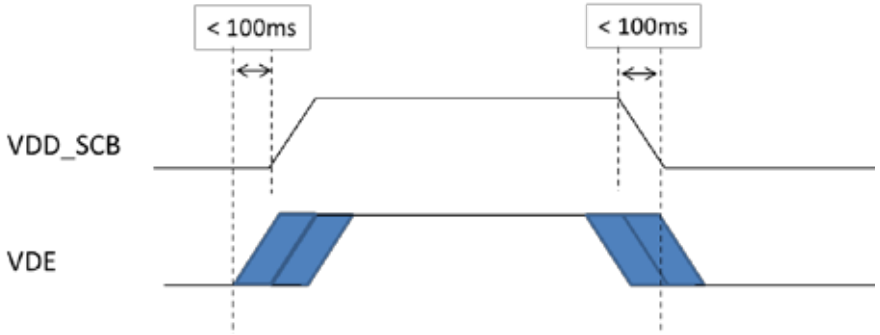


Figure 4-7: Order of turning ON/OFF power supplies for EMMC

The speed of powering on (the time for getting to full amplitude) should be 50us or above.

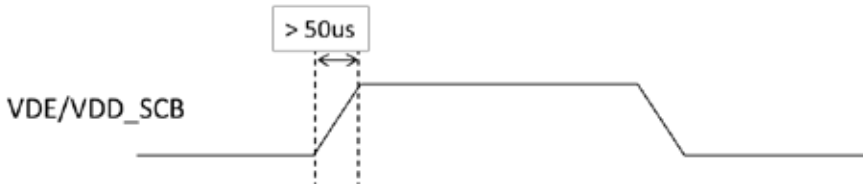


Figure 4-8: Speed of turning ON power supplies for EMMC

4.1.6. FPDLink

The power supplies should be turned on/off in the following order.
Powering on: VDD_FPD→VDE_FPD
Powering off: VDE_FPD→VDD_FPD
If the above order of turning on/off power supplies cannot be observed, the interval between turning on and turning off should be 100ms or below.

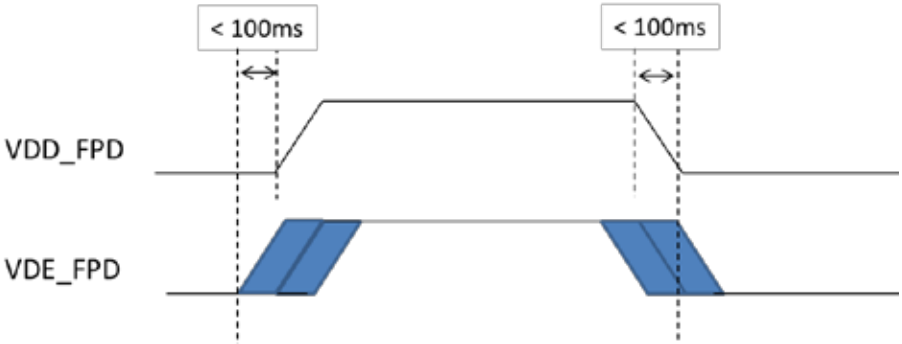


Figure 4-9: Order of turning ON/OFF power supplies for FPDLink

The speed of powering on (the time for getting to full amplitude) should be 50us or above.

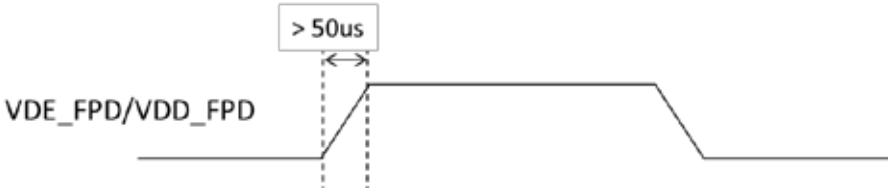


Figure 4-10: Speed of turning ON power supplies for FPDLink

4.1.7. USB3.0

The power supplies should be turned on/off in the following order.

Powering on: VDD_SCB→VDU/VDN/AVDF1/AVDP→AVD18→AVDF1

Powering off: AVDF1→AVD18→VDU/VDN/AVDF1/AVDP→VDD_SCB

* The order of turning on/off VDU/VDN/AVDF1/AVDP power supplies is not specified.

If the above order of turning on/off power supplies cannot be observed, the interval between turning on and turning off should be 200ms or below.

Caution) Because PHY goes into uncontrolled state while the external (except VDD_SCB) power supplies are ON and the internal (VDD_SCB) power supply is OFF, signals may be output to the outside (USB bus of PHY). And there is no guarantee that these signals are compliant with USB3.0 standard.

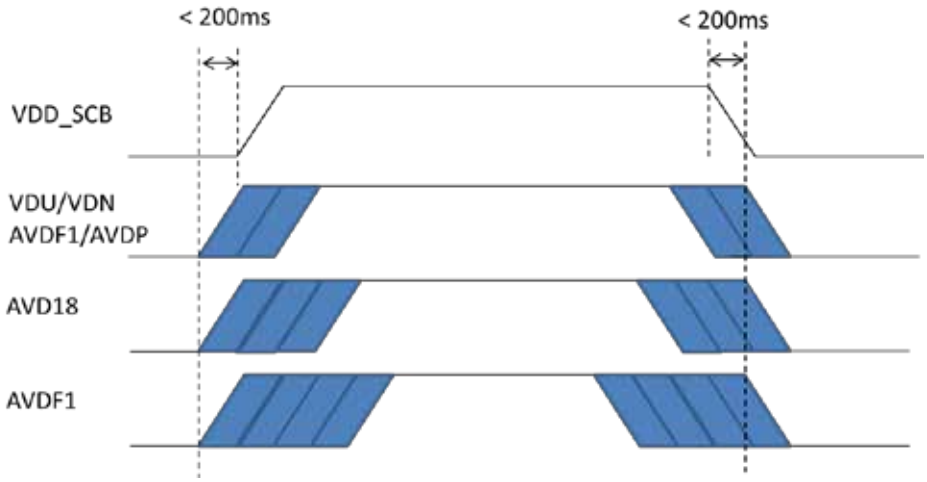


Figure 4-11: Order of turning ON/OFF power supplies for USB3.0

4.1.8. USB2.0

The power supplies should be turned on/off in the following order.

Powering on: VDD_SCB→AVDF1/AVDP→AVD18→AVDF1

Powering off: AVDF1→AVD18→AVDF1/AVDP→VDD_SCB

* The order of turning on/off AVDF1/AVDP power supplies is not specified.

If the above order of turning on/off power supplies cannot be observed, the interval between turning on and turning off should be 200ms or below.

Caution) Because PHY goes into uncontrolled state while the external (except VDD_SCB) power supplies are ON and the internal (VDD_SCB) power supply is OFF, signals may be output to the outside (USB bus of PHY). And there is no guarantee that these signals are compliant with USB2.0 standard.

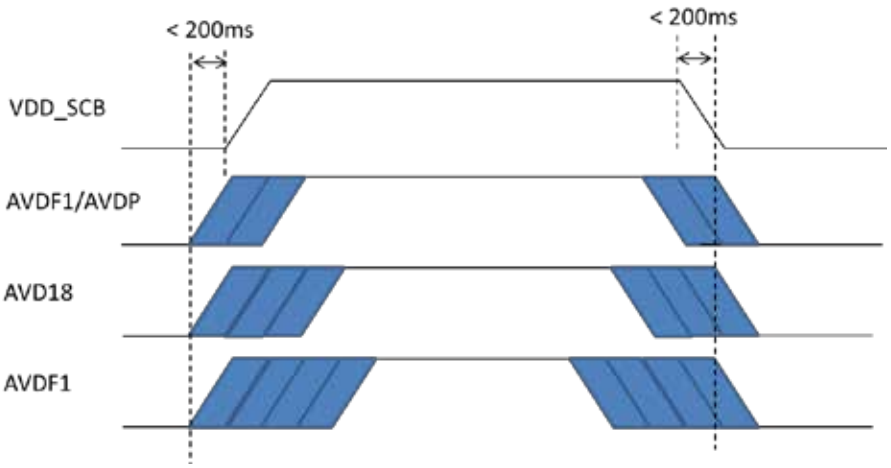


Figure 4-12: Order of turning ON/OFF power supplies for USB2.0

4.1.9. PCIE

The power supplies should be turned on/off in the following order.
Powering on: VDD_SCB→VPTX_PCIE/VP_PCIE→VPH_PCIE
Powering off: VPH_PCIE→VPTX_PCIE/VP_PCIE→VDD_SCB
* The order of turning on/off VPTX_PCIE/VP_PCIE power supplies is not specified.

If the above order of turning on/off power supplies cannot be observed, the interval between turning on and turning off should be 100ms or below.

Caution) Because PHY goes into uncontrolled state while the external (except VDD_SCB) power supplies are ON and the internal (VDD_SCB) power supply is OFF, signals may be output to the outside (PCIE bus of PHY). And there is no guarantee that these signals are compliant with PCIE standard.

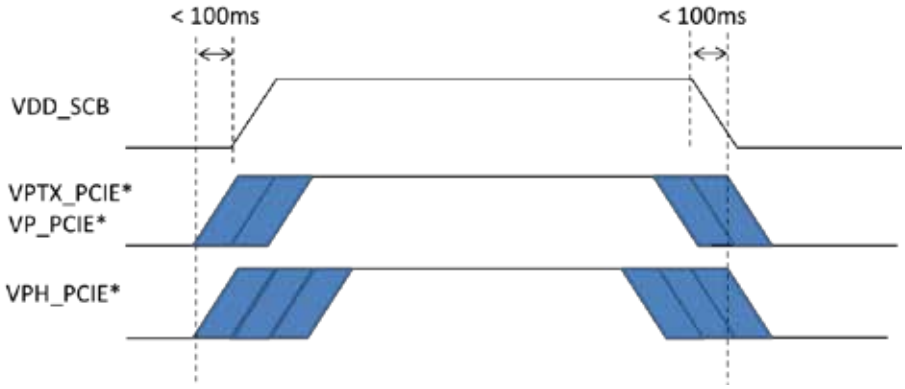


Figure 4-13: Order of turning ON/OFF power supplies for PCIE

4.1.10. DDR

The power supplies should be turned on/off in the following order.
Powering on: VDD→VAA_PLL1/VAA_PLL2→VDE15/VDE15A
Powering off: VDE15/VDE15A→VAA_PLL1/VAA_PLL2→VDD
* The order of turning on/off VAA_PLL1/VAA_PLL2 power supplies is not specified.

Turn on VAA_PLL within 0ms to 100ms after beginning to turn on VDD.
Turn off VDD within 0ms to 100ms after beginning to turn off VAA_PLL.
The order of turning on/off VDE15/VDE15A power supplies is not specified.

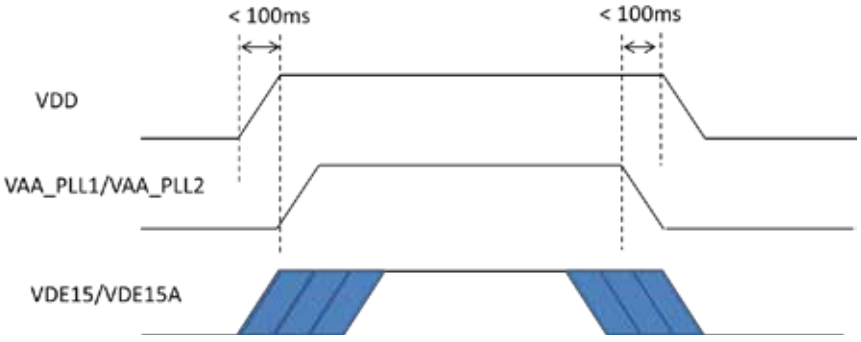


Figure 4-14: Order of turning ON/OFF power supplies for DDR

The speed in powering on (the time for getting to full amplitude) should be 10us or above.

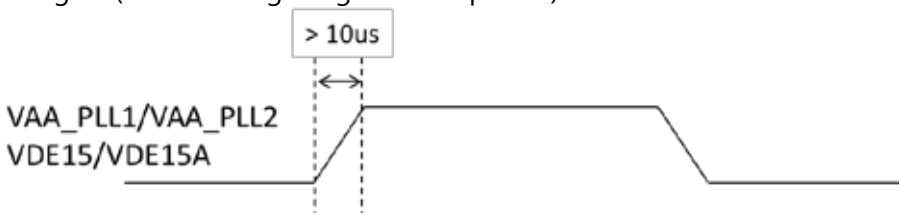


Figure 4-15: Speed of turning ON power supplies for DDR

4.1.11. Other than Above

The power supplies should be turned on/off in the following order.

Powering on: VDDI→VDDE

Powering off: VDDE→VDDI

* For power supply names of VDDI/VDDE, see 2.3Pin Information.

If the above order of turning on/off power supplies cannot be observed, the interval between turning on and turning off should be 100ms or below.

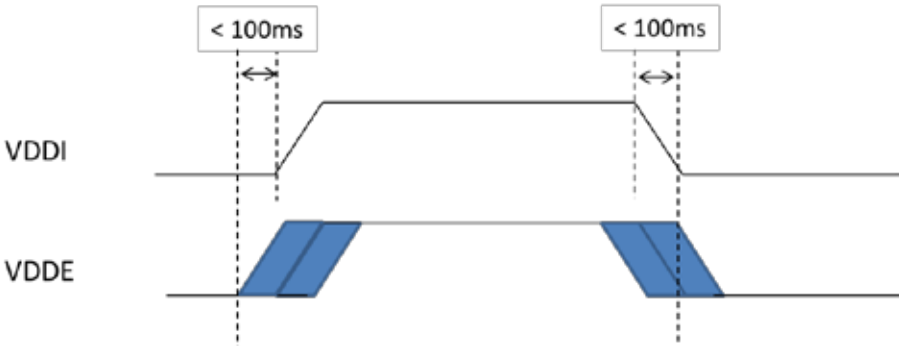


Figure 4-16: Order of turning ON/OFF power supplies for Others

The speed of powering on (the time for getting to full amplitude) should be 50us or above.

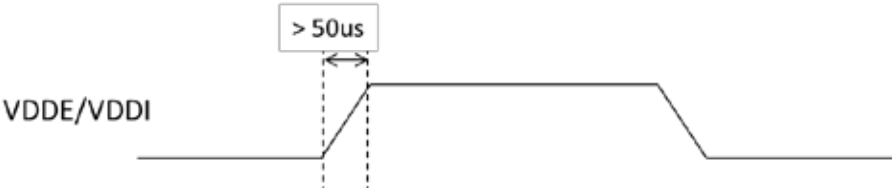


Figure 4-17: Speed of turning ON power supplies for Others

4.2. Order of Turning ON/OFF VDDE-VDDE Power Supplies

The order of turning on/off VDDE power supplies is not stipulated.
Caution) When VDE15 power supply is ON, VDE15A should be also ON.

4.3. Order of Turning ON/OFF VDDI-VDDI Power Supplies

The power supplies should be turned on/off in the following order.
Powering on: VDDA→VDD_SCB→VDD
Powering off: VDD→VDD_SCB→VDDA
If the above order of turning on/off power supplies cannot be observed, perform reset to initialize circuits.

5. Pin Handling

5.1. SDIO0/SDIO1

- Connect the following 0.22uF external capacitances between BIAS pins (VNODE, VBIASP/VBIASN/VBIASPEXT/VBIASNEXT).

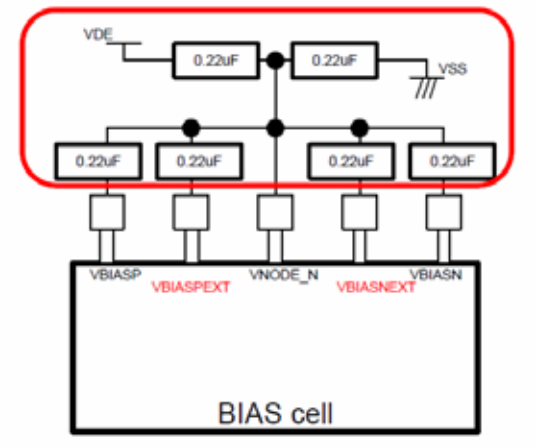


Figure 5-1: Pin handling of SDIO0/1

5.2. USB2.0/3.0

- EXT12K should be connected to GND via an External 12K[ohm] resistive element. The terminal of external resistor should be arranged near the pin and the line between the pin and the resistor should be as short as possible. Use a resistive element whose accuracy is 12KΩ±1%.

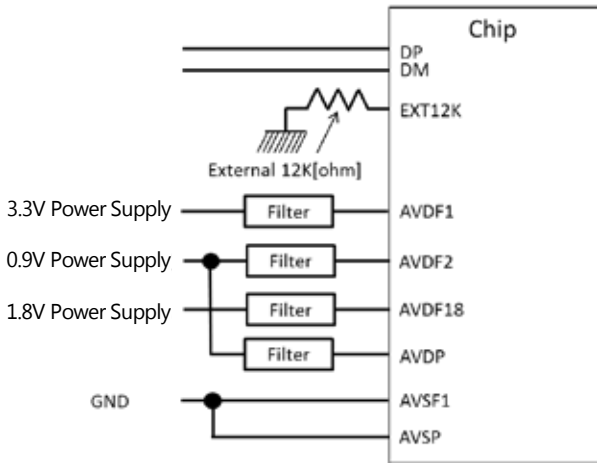


Figure 5-2: Pin handling of USB2.0/3.0

5.3. PCIE

- REFRES_I should be connected to GND via a 200Ω resistive element. The terminal of external resistor should be arranged near the pin and the line between the pin and the resistor should be as short as possible. Use a resistive element whose accuracy is 200Ω±1%±100ppm/°C.

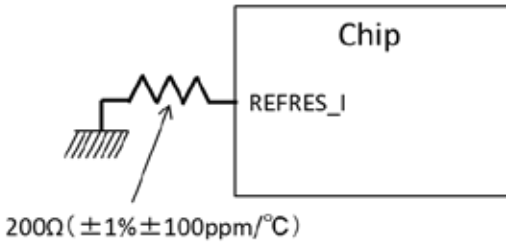


Figure 5-3: Pin handling of PCIE

5.4. DDR

- Noise carried on VAA_PLL (analog power supply of PLL) might increase Jitter to prevent its characteristics from being satisfied. Use a 75-150Ω ferrite bead to reduce impedance. Place 10uF, 1uF, and 0.1uF, which should be the nearest to the package.

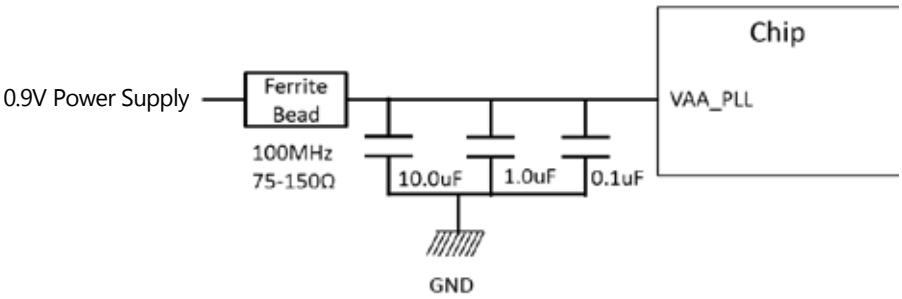


Figure 5-4: Pin handling of DDR 1

- MVREF should track the variation in the DC value of VDE15, so it should be constructed using resistors and capacitors. MVREF requires dynamic noise to be limited to ±2%. Leave a space (for five signals) between MVREF and a signal so as not to be affected by noise from the signal. And the line width should be 510um or above in order to minimize DC drop.

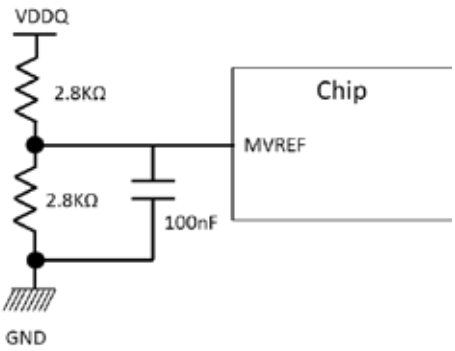


Figure 5-5: Pin handling of DDR 2

6. Important Notes

6.1. On the Handling of Pins when the High Speed Interface is Not Used

・ When the High Speed interface is not used, it is possible to reduce the power consumption by switching OFF the power supply being used. The handling of the pins when this interface is not used is described here.

6.1.1. PCI-express #0

Table 6-1: Pin handling when PCIe#0 is not used

Signal/Power/GND	Handling when not used
PCIE0_REFRES_I	OPEN
PCIE0_TXPO3	
PCIE0_TXPO2	
PCIE0_TXPO1	
PCIE0_TXPO0	
PCIE0_TXNO3	
PCIE0_TXNO2	
PCIE0_TXNO1	
PCIE0_TXNO0	
XPCIE0_PERST	
PCIE0_REFCLKPI	GND
PCIE0_REFCLKMI	
PCIE0_RXPI3	
PCIE0_RXPI2	
PCIE0_RXPI1	
PCIE0_RXPI0	
PCIE0_RXNI3	
PCIE0_RXNI2	
PCIE0_RXNI1	
PCIE0_RXNI0	
VPTX_PCIE0	
VPH_PCIE0	
VP_PCIE0	
GD_PCIE	
PCIE0_PRVRETYPEI	

6.1.2. PCI-express #1

Table 6-2: Pin handling when PCIe#1 is not used

Signal/Power/GND	Handling when not used
PCIE1_REFRES_I	OPEN
PCIE1_TXPO3	
PCIE1_TXPO2	
PCIE1_TXPO1	
PCIE1_TXPO0	
PCIE1_TXNO3	
PCIE1_TXNO2	
PCIE1_TXNO1	
PCIE1_TXNO0	
XPCIE1_PERST	
PCIE1_REFCLKPI	GND
PCIE1_REFCLKMI	
PCIE1_RXPI3	
PCIE1_RXPI2	
PCIE1_RXPI1	
PCIE1_RXPI0	
PCIE1_RXNI3	
PCIE1_RXNI2	
PCIE1_RXNI1	
PCIE1_RXNI0	
VPTX_PCIE1	
VPH_PCIE1	
VP_PCIE1	
GD_PCIE	
PCIE1_PRVRETYPEI	

6.1.3. USB3.0 Host #0

・ If USB3.0 Host #0 is not used, USB3.0 Host #1 is unavailable. Note that USB3.0 Host #1 is also handled similarly to when it is not used.

Table 6-3: Pin handling when USB3.0 Host #0 is not used

Signal/Power/GND	Handling when not used
USB30_SSEARXIP	OPEN
USB30_SSEARXIN	
USB30_SSEXTXOP	
USB30_SSEXTXON	
USB30_OVERCRNT	
USB30_VBUSCTRL	
USB30_HSDP	
USB30_HSDM	
USB30_HSEXT12K	
USB3_REFCLK	GND
VSU_USB30	
VDU_USB30	
VDN_USB30	
VSN_USB30	
AVDF1_USB30	
AVDF2_USB30	
AVDP_USB30	
AVSP_USB30	
AVS_USB30	
AVD18_USB30	

6.1.4. USB3.0 Host #1

Table 6-4: Pin handling when USB3.0 Host #1 is not used

Signal/Power/GND	Handling when not used
USB31_SSEARXIP	OPEN
USB31_SSEARXIN	
USB31_SSEXTXOP	
USB31_SSEXTXON	
USB31_OVERCRNT	
USB31_VBUSCTRL	
USB31_HSDP	
USB31_HSDM	
USB31_HSEXT12K	
VSU_USB31	GND
VDU_USB31	
VDN_USB31	
VSN_USB31	
AVDF1_USB31	
AVDF2_USB31	
AVDP_USB31	
AVSP_USB31	
AVS_USB31	
AVD18_USB31	

6.1.5. USB2.0 Host

Table 6-5: Pin handling when USB2.0 Host is not used

Signal	Handling when not used
USB2H_DP	OPEN
USB2H_DM	
USB2H_EXT12K	
USB2H_PRTPWRO	
AVDF1_USB2H	GND
AVDF2_USB2H	
AVDP_USB2H	
AVSP_USB2H	
AVS_USB2H	
AVD18_USB2H	
XUSB2H_OVCRNTI	VDE

6.1.6. USB2.0 Host/Device

Table 6-6: Pin handling when USB2.0 Host/Device is not used

Signal	Handling when not used
USB2D_DP	OPEN
USB2D_DM	
USB2D_EXT12K	
USB2D_PRTPWRO	
USB2D_DPUO	
AVDF1_USB2HDC	GND
AVDF2_USB2HDC	
AVDP_USB2HDC	
AVSP_USB2HDC	
AVS_USB2HDC	
AVD18_USB2HDC	
USB2D_VBUSVALI	
XUSB2D_OVCRNTI	VDE
USB2D_IDDIGI	

6.2. On the Handling of Pins When the Different Interfaces are Not Used

Table 6-7: Handling of pins when the different interfaces are not used (1)

Category	Signal	Handling when not used
JTAG	TCK	OPEN
	TMS	
	TDI	
	XTRST	
	TDO	
GPIO	PD[65:0]	OPEN
UART	SIN0	
	SOUT0	
	XCTS0	
	XRTS0	
I2C	I2C0_SCL	Pull-up(VDE)
	I2C0_SDA	
	I2C1_SCL	
	I2C1_SDA	
	I2C3_SCL	
	I2C3_SDA	
Ether MAC RGMII	ET_GTXCLK	OPEN
	ET_TXD[3:0]	
	ET_TXEN	
	ET_MDCLK	
	ET_PME	
	ET_INT	
	ET_RXCLK	GND
	ET_RXD[3:0]	
	ET_RXDV	
	ET_MDIO	
HSSPI	HSSPI_CSO[1:0]	OPEN
	HSSPI_CLK	
	HSSPI_DAT[3:0]	
I2S	I2S_ECLK	OPEN
	I2S_SCLK	
	I2S0_FSYN	
	I2S0_SDO	
	I2S1_FSYN	
	I2S1_SDO	

Table 6-8: Handling of pins when the different interfaces are not used (2)

Category	Signal	Handling when not used
SDIO	SDIO[1:0]_CLK	OPEN
	SDIO[1:0]_CMD	
	SDIO[1:0]_DAT[3:0]	
	VBIASP[1:0]	GND
	VBIASN[1:0]	
	VBIASPEXT[1:0]	
	VBIASNEXT[1:0]	
	VNODE_N[1:0]	
	VDE_SDIO[1:0]	
	SDIO[1:0]_CD	
	SDIO[1:0]_WP	
	SDIO[1:0]_PWR0	OPEN
	SDIO[1:0]_PWRERR	GND
	SDIO[1:0]_VSEL	OPEN
FPDLink	FPD_CLKP	OPEN
	FPD_DATP[3:0]	
	FPD_CLKN	
	FPD_DATN[3:0]	

7. Cautions for Handling

Semiconductor devices fail at certain probabilistic rates. Also failures of semiconductor devices are greatly affected by conditions (circuit condition, environment condition, etc.) under which they are used.

The following describes what must be taken care of and taken into consideration in order to use semiconductor devices in a higher reliable state.

7.1. Cautions for Designing

This Section describes what should be taken care of for designing electronic equipment using semiconductor devices.

7.1.1. Complying with Absolute Maximum Ratings

Application of an excessive stress (voltage, current, temperature, etc.) is likely to destroy semiconductor devices. What define these limiting values are absolute maximum ratings. Therefore, take care so that not even one parameter exceeds the ratings.

7.1.2. Complying with Recommended Operating Conditions

The recommended operating conditions are the ones that guarantee normal operation of semiconductor devices. All of the standard values for electrical characteristics are guaranteed within the scope of these conditions. Always use devices under the recommended operating conditions. When devices are used beyond these conditions, their reliability might be affected negatively.

It is not guaranteed to use devices with the items, conditions for use, and logical combinations which are not described in this document. If you want to use them under the conditions not described here, be sure to contact our sales department beforehand.

7.1.3. Handling and Protection of Pins

Semiconductor devices have power supplies and various input/output pins. The following cautions are required for these.

1. Prevention of overvoltage and overcurrent
   Application of voltage or current beyond maximum ratings excessive to each pin causes degradation inside devices and in the worst case leads to destruction. When designing equipment, prevent the generation of such overvoltage and overcurrent.
2. Protection of output pins
   If output pins are short-circuited with power supply pins or other output pins, or connected to large capacity load, a large current might flow. Because devices are degraded if this state lasts for a long time, such connection should not be made.
3. Handling of unused input pins
   If an input pin with very high impedance is used while it is open, its operation might be unstable. It should be connected to a power supply pin or a ground pin via an appropriate resistor.

7.1.4. Latchup

Semiconductor devices are configured by forming P-type and N-type areas on boards. If abnormal voltage is applied from the outside, an internal parasitic PNPN joint (thyristor structure) might conduct and a large current exceeding several hundred mA might continue to flow to power supply pins. This is called latchup. This phenomenon is likely to not only degrade the reliability of a device but also lead to its destruction and generation of heat, smoke, and fire. To prevent this, the following should be noticed.

1. Be sure not to apply voltage exceeding the maximum rating to pins. Take notice of abnormal noise, surge, etc. as well.
2. Consider the sequence for turning on power supplies to prevent an abnormal current from flowing.

7.1.5. Complying with Regulations and Standards for Security or the like

All the countries of the world establish various regulations and standards for security, electromagnetic interference, and so on. Please conform equipment to these regulations and standards when designing them.

7.1.6. Fail-Safe Design

Failures of semiconductor devices occur at certain probabilistic rates. We would like you to carry out safety designs such as equipment redundancy design, fire spreading countermeasure design, overcurrent prevention design, wrong operation prevention design, etc., so that, even if a semiconductor device fails, as a result human injury accidents, fire accidents, and accidents causing social damage do not occur.

7.1.7. Cautions regarding Applications

Products described in this document have been designed and manufactured for general use such as industrial applications, office work, and personal/home use. These are not designed and manufactured, when very high safety is required, and the said safety is not secured temporarily, for the use (such as nuclear reaction control in nuclear power facility, operation control in aircraft automatic flight control, air traffic control, and operation control in mass transport system, medical equipment for life support, and missile launch control in weapon system) which has a critical influence on society, and is associated directly with grave danger to life and body, and for the use (such as submarine repeater, and space satellite) which requires very high reliability. Please note that our company does not bear any liabilities whatsoever regarding damages arising out of use for these applications.

7.2. Cautions for Implementing Packages

The quality assurance for heat resisting property on soldering is applied only to the implementations in accordance with the conditions which our company recommends. For more information about conditions for implementation, contact our sales department.

7.2.1. Lead-Free Package

Note that if Sn-Ag-Cu type ball of BGA package is implemented in Sn-Pb eutectic solder, bonding strength can decrease according to usage.

7.2.2. On the Storage of Semiconductor Devices

Packages absorb moisture if they are left in the natural environment. The following should be noticed.

1. Condensation of water occurs on a product in an environment where temperature changes drastically. Avoid such an environment and store it in a place where temperature changes are few.
2. We recommend using dry boxes for the storage location of products. Store them with relative humidity of 60%RH or below and a temperature of 5°C to 30°C.
3. Our company uses aluminum laminate bags with high moisture-proof property for packaging material of semiconductor devices and silica gel for desiccant, as necessary. Store semiconductor devices sealed in aluminum laminate bags.
4. Avoid locations where corrosive gas is generated and where there is much dust.

7.2.3. On Baking

Packages absorbing moisture can be dehumidified by performing baking (heating treatment).

7.2.4. Static Electricity

Note the following, because semiconductor devices are liable to be destroyed due to static electricity.

1. The relative humidity of working environment should be 40% to 60%RH.
   Consider the use of static eliminators (ion generators) or the like, as necessary.
2. Conveyors, soldering ports, soldering irons, and peripheral incidental facilities to use should be grounded to the earth.
3. To prevent electrification of a human body, electrification charges should be kept to the minimum, by grounding to the earth with high resistance (around 1MΩ) through a ring, bracelet or the like, by wearing conductive clothes and shoes, by laying a conductive mat on a floor, and so on.
4. Grounding or anti-static treatment should be conducted to jigs and instruments.
5. Do not use materials liable to be electrically charged such as expanded polystyrene when storing assembled and completed boards.

7.3. Cautions regarding Operating Environment

The reliability of semiconductor devices is dependent on ambient temperature and other environmental conditions described above. Note the following when using devices.

1. Humidity environment
   If devices are used under high humidity environment for a long time, malfunction with leak property can occur on not only devices themselves but also printed circuit boards and so on. Make consideration such as conducting moisture-proof treatment when high humidity is anticipated.
2. Electrostatic discharge
   If there is something charged at high voltage right near a semiconductor device, discharge might be generated to cause malfunction. In this case, take measures to prevent static electricity or electric discharge.
3. Corrosive gas, dust, and oil
   If devices are used in corrosive gas atmosphere or with dust, oil, and so on adhering to them, a chemical reaction might affect the devices negatively. When using them under such an environment, consider preventive measures.
4. Radial rays and cosmic rays
   Common devices do not assume in design an environment where they are exposed to radial rays or cosmic rays. Therefore, shield devices from these rays when using them.
5. Smoking and firing
   Do not use devices near combustibles. When smoking or firing, toxic gas might be generated.

Consult our sales department if you want to use devices under other peculiar environments.